AN AREA-EFFICIENT PARTIALLY RECONFIGURABLE CROSSBAR SWITCH WITH LOW RECONFIGURATION DELAY

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MOTIVATION

- Multiprocessors on the rise (MPSoCs)
  - Single processor systems unavailable to meet application performance requirements
  - Multiple processors + Memory + IO devices
  - Bottleneck shifts from computation to communication
- Networks-on-Chip (NoCs) proposed
  - Bus is not scalable
MOTIVATION

- MPSoCs need to handle multiple use cases – combinations of multiple applications
- Use cases have different connectivity requirements
- NoCs have to be dynamically reconfigurable and provide guaranteed throughput: TDM vs SDM
TDM vs SDM

TDM

Node 1

Node 2

CCBA

SDM

Node 1

Node 2

A
B
C
MOTIVATION

- Two approaches to dynamic reconfiguration of NoC
  - Adding reconfiguration logic
    - Incurs area overhead
  - Partial reconfiguration (PR)
    - High reconfiguration delay
    - Requires large storage space
    - Caters to predefined use cases only
CONTRIBUTIONS

- Problem lies with the design of crossbar switch
- A novel partially reconfigurable crossbar switch design is proposed
  - 84% area saving!
  - 78% reconfiguration delay reduction!
  - Runtime bit-stream generation
  - Glitch-free reconfiguration
CROSSBAR SWITCH ARCHITECTURE
MULTIPLEXER AS BUILDING BLOCK OF CROSSBAR SWITCH
A Configurable Logic Block (CLB)
LUT AS MULTIPLEXER

- Conventional LUT multiplexer
  - Requires $\log_2 N$ selector pins for $N$ data inputs

- PR based LUT multiplexer
  - Requires no dedicated selector pins
  - Selection is done by changing LUT content through PR
  - Allows larger multiplexer to be built with the same number of LUTs
LUT AS MULTIPLEXER

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**SCALABLE APPROACH**

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![Diagram of logic gate]
DESIGN FLOW

Network specification in HDL

System specification in HDL

Logic synthesis

Placement and routing

Bitstream generation

Placement constraints
RUNTIME BITSTREAM GENERATION & RECONFIGURATION

LUT configuration database

ICAP

14
MINIMIZING RECONFIGURATION DELAY

- Apply AREA_GROUP constraint to limit the placement of LUT to the minimum number of CLB columns required
- Identify the frames that are responsible for LUT content
  - 8 out of 36 frames are required
  - 78% speedup!
- Use the Multiple Frame Write (MFW) command of ICAP
**Multiple Frame Write (MFW)**

2 LUTs configured *identically* by transferring the configuration data only *once*!
GLITCH-FREE CONNECTION ESTABLISHMENT

Configuration of first router is unchanged

Operation of first router is unaffected
RESULTS AND ANALYSIS
Area saving of PR router – single link

![Graph showing area saving comparison between conventional and PR based multiplexers.]
Area savings of PR router

![Graph showing area savings comparison between Non-PR and PR routers. The graph displays the area (in terms of number of LUTs) for each router type, with a breakdown between routing logic and control logic.]
AREA REQUIREMENT OF VARIOUS NETWORK TOPOLOGIES

![Graph showing area requirement of various network topologies](image-url)
CONCLUSIONS

A novel partially reconfigurable crossbar switch design has been presented

- 84% area saving!
- 78% reconfiguration delay reduction!
- Runtime bitstream generation
- Glitch-free reconfiguration
QUESTIONS?