Hardware Implementation of Stereo Correspondence Algorithm for the Exomars Mission

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1. Objectives

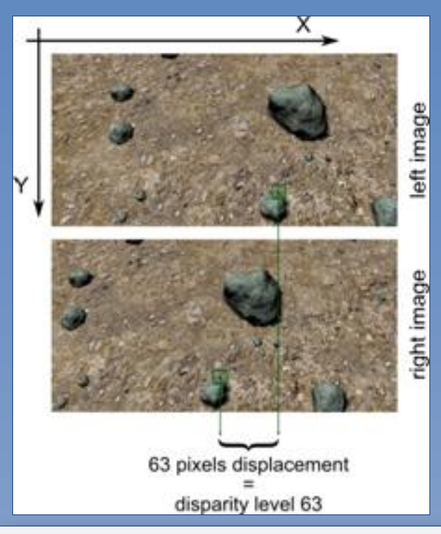
- VHDL implementation of a stereo correspondence algorithm for rover navigation
- Design toolset for supporting the HW/SW co-design methodology
- Architecture Design Space Exploration

Target Device:

- Xilinx Virtex-6 (LX240T-FF1759)

Application Domain:

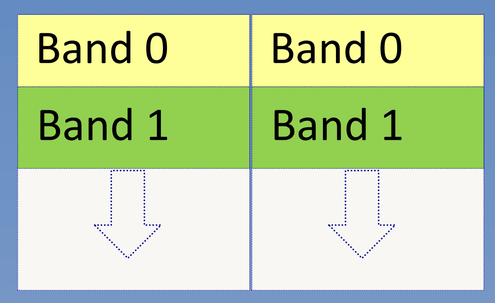
- Autonomous robotics navigation
- Disparity map generation
- SLAM (Simultaneous Localization and Map reconstruction)

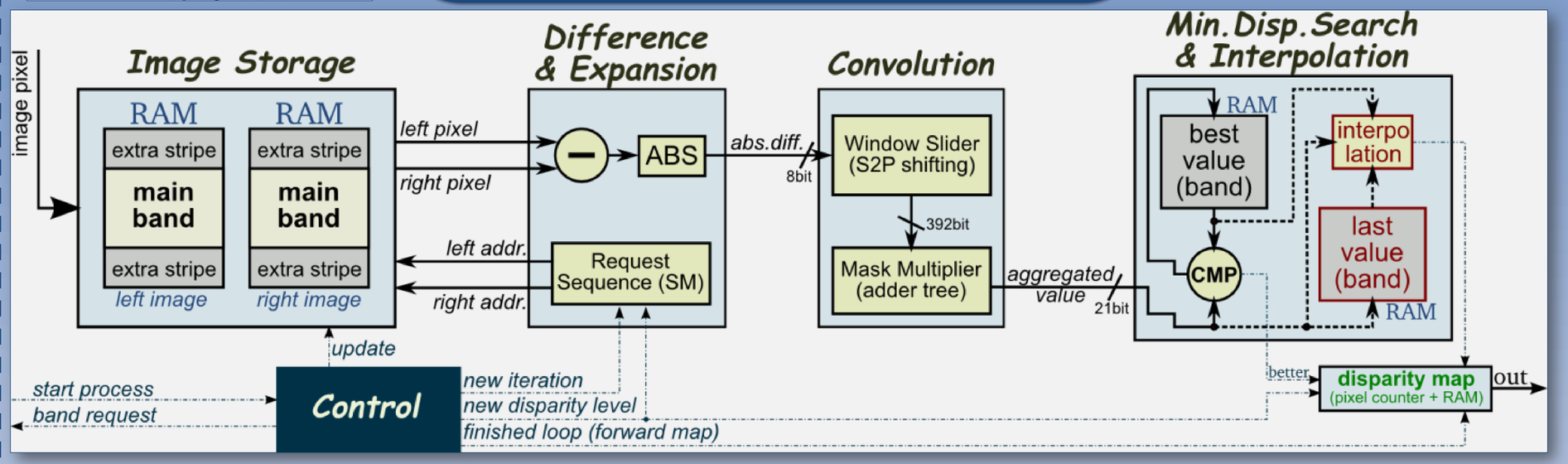


3. Architecture of Disparity Module

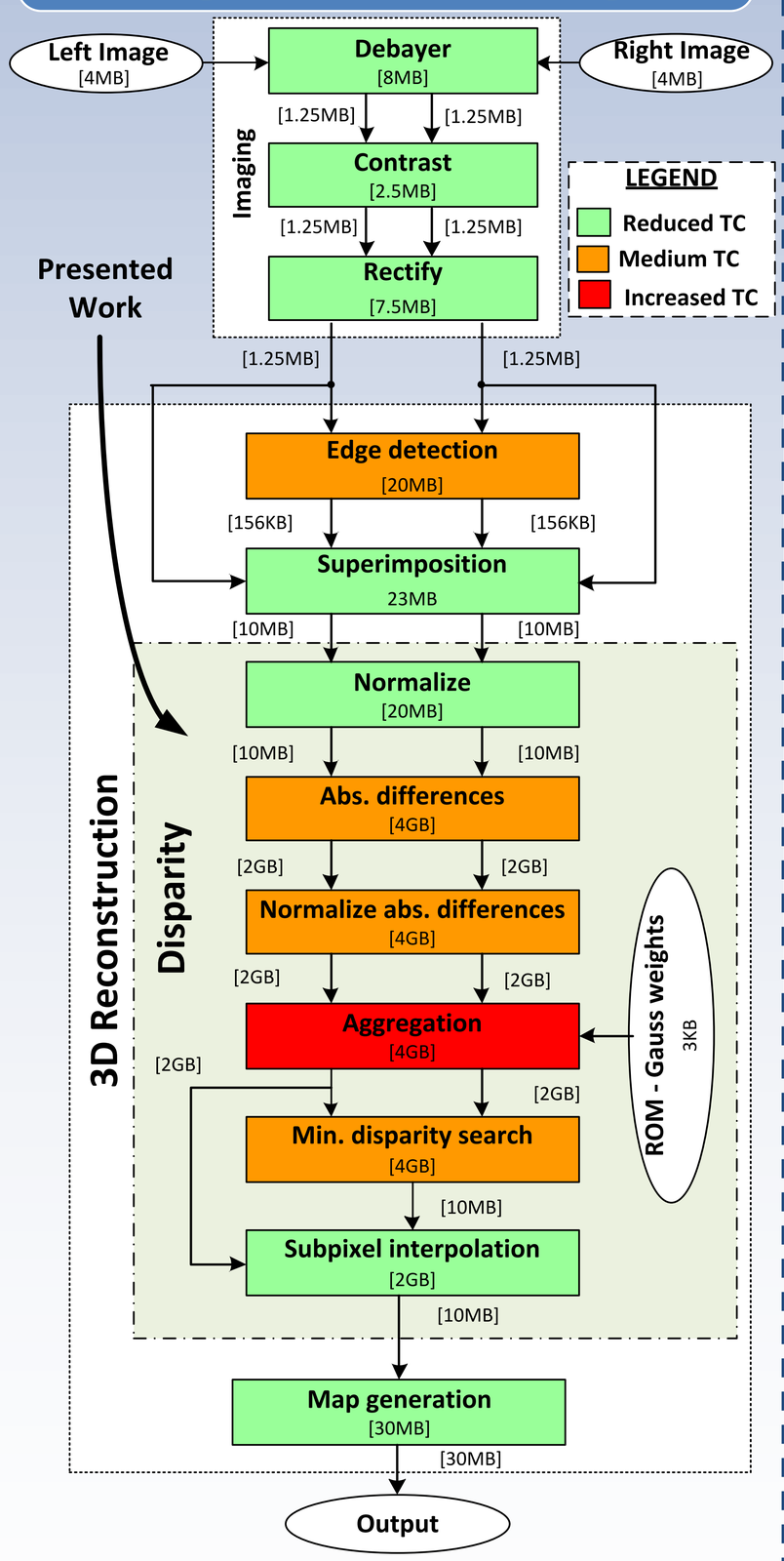
Implementation Optimizations

- Division of image in bands
- Sequential processing of bands
- Compute one disparity level per iteration
- Parallelize convolution (mask multiplication)
- Extensive pipelining from image memory to disparity memory
  - ➢ throughput: one pixel per cycle
  - ➢ effectively, dozens of pixels processed in parallel





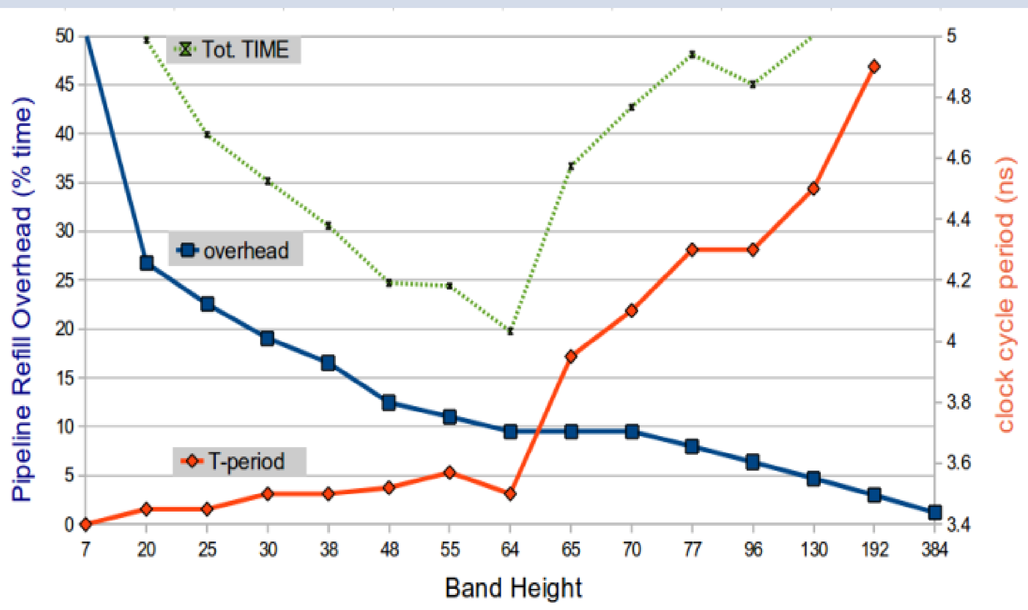
2. Spartan System: Algorithm's Profiling



Architecture details

- The first component stores the image pixels
- The remaining three comprise the datapath of the Disparity module
- The datapath is implemented as a long pipeline (dozens of stages, configured at compile time) starting from the image memory and terminating at the disparity map memory.

Design Space Architecture Exploration



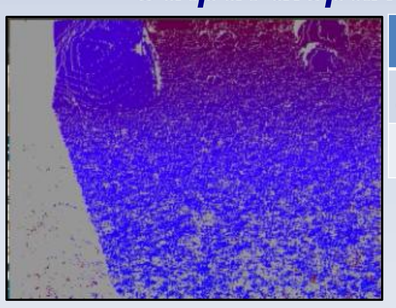
Architecture Trade-offs

- The hardware cost increases monotonically with the band height due to the increase of the internal memories and the wide datapaths addressing these memories.
- Execution time changes non-monotonically with the band height: given as a function of height, TIME (height), it produces a curve with local minima.
- Band height causes two different quantities to reduce and have opposite impact on TIME: the operating frequency and the pipeline refill overhead.

4. Implementation

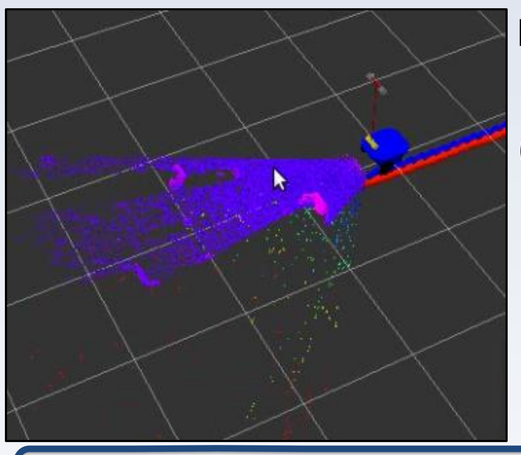
Input image stereo pair (1120x1120)

Output disparity map



	Time	Mem.
SW	1h	4GB
HW	2.3sec	0.4MB

Speedup 1,565x



Execution on ROS

(diamondback)

rviz package

Max. operating frequency = 283 MHz

Component	Slices	LUTs	Registers	RAM Blocks
Image Storage	73	195	229	32
Difference & Expansion	106	327	92	0
Convolution	603	1,910	1,952	7
MDS & Interpolation	206	586	843	62
Control	10	21	18	0
Total	**998**	**2,978**	**3,116**	**101**

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