DESIGN SPACE EXPLORATION FOR AUTOMATICALLY GENERATED CRYPTOGRAPHIC HARDWARE USING FUNCTIONAL LANGUAGES

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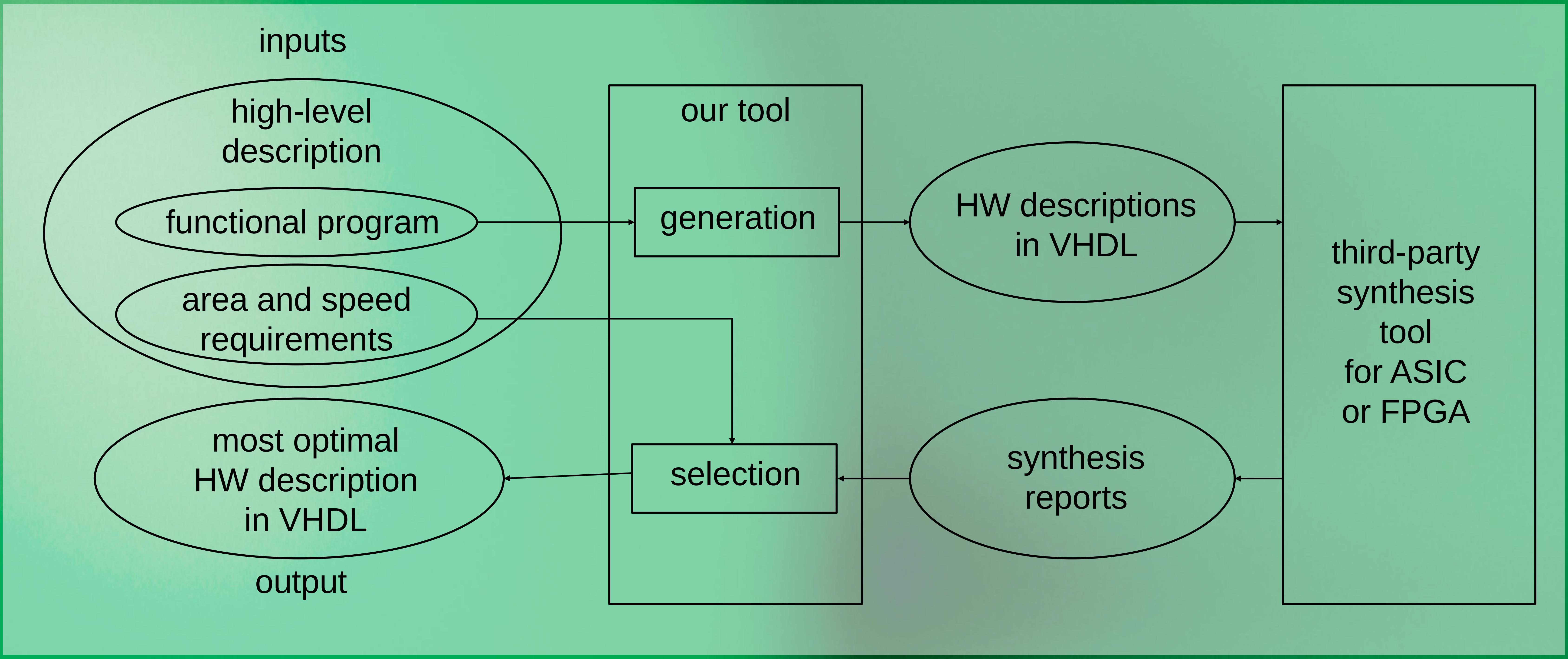
Goals:

- EDA tool for the automatic generation of cryptographic hardware in VHDL
- taking into account user requirements by design space exploration



Results:

- listing features for design space exploration
  - exploration in the generation phase
  - exploration in the synthesis phase (by exploring options of synthesis tool)
- data path example: 192-bit adder → 32 automatically generated architectures
- control logic example: AES controller → 18 automatically generated architectures

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