Fast and Accurate Single Bit Error Injection into SRAM Based FPGAs

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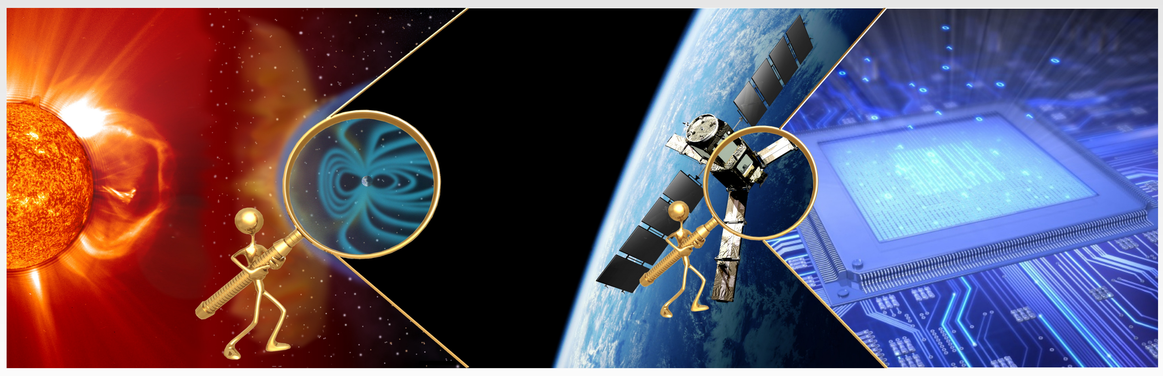
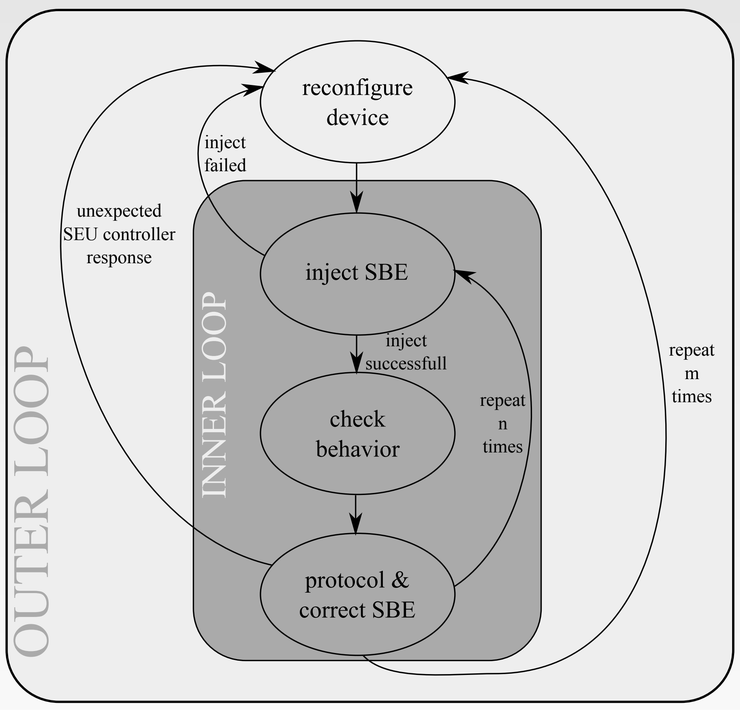
Introduction



When impacting the silicon of an integrated circuit heavy ions, protons and other kinds of radiation can lead to single effects. These single effects are changes in the logic of some connections and can lead to wrong system behaviour.

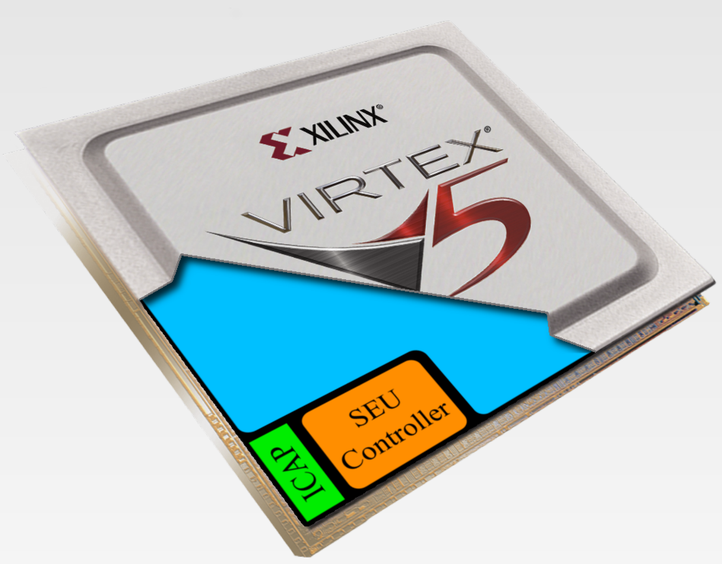
For critical applications the consequences of this need to be considered, which requires a fault emulation strategy. Many fault injection strategies today base either on external or internal reconfiguration, where each of the two has different strengths.

SBE test flow



Complete reconfiguration in the outer loop results in a high accuracy, the fast partial reconfiguration in the inner loop leads to fast SBE emulation times for SBE test flow execution.

Accuracy estimation



The accuracy of this flow is strongly dependent on the frequency of SBE side effects to happen. SBE side effects occur when bits of the ICAP manipulation logic get affected by injection of errors. The probability of this situation to occur is small and can be estimated as follows.

P_{sSeu} is the probability of the n-th injection result to be side-effect free.

$$P_{sSEU} = \frac{1}{n}\sum_{k=1}^{n}(1\text{-}\frac{B_{con}p_{ctr}}{B_{dev}})^k$$

For time redundant results P^{μ}_{SEU} is the probability of the voted result to be side effect free.

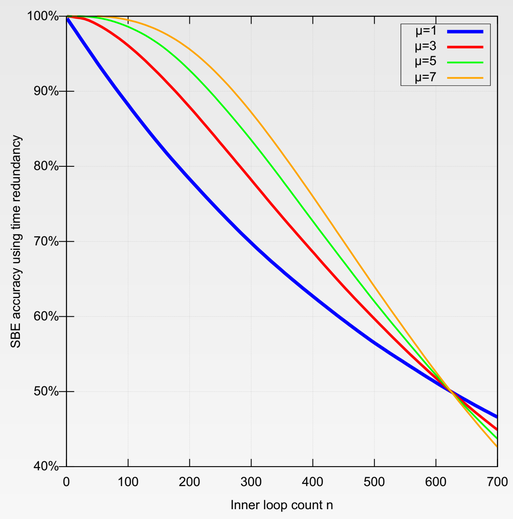
$$P^{\mu}_{SEU} = \sum_{\substack{x=\lceil \mu/2 \rceil \\ x\in\mathbb{N}}}^{\mu} \binom{\mu}{x} P^{x}_{sSEU}(1-P_{sSEU})^{\mu-x}$$

For example $\mu = 3$:

$$P^{3}_{SEU} = \underbrace{\binom{3}{2} P^{2}_{sSEU}(1-P_{sSEU})}_{2\ tests\ correct} + \underbrace{P^{3}_{sSEU}}_{3\ tests\ correct}$$

Effect of time redundancy

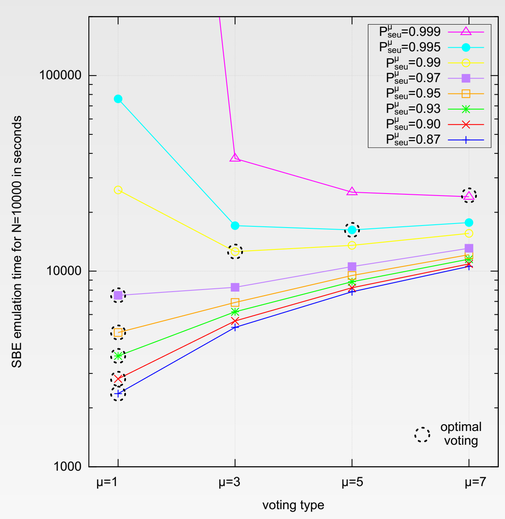
Accuracy for different μ



Temporal redundancy has a significant positive impact on the accuracy of the SBE test flows results. Using redundancy the achievable maximum inner loop count grows significantly.

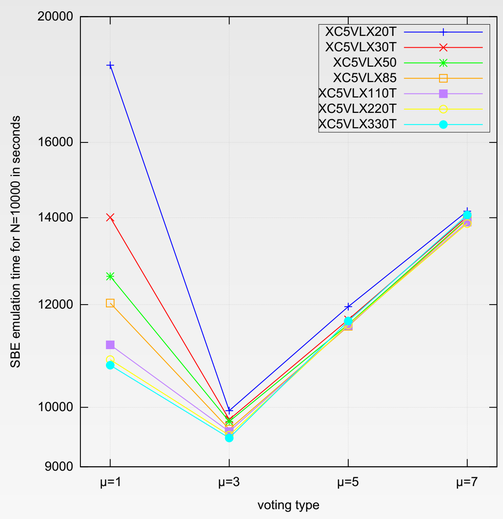
Speed accuracy tradeoffs

Optimal voting (accuracy)



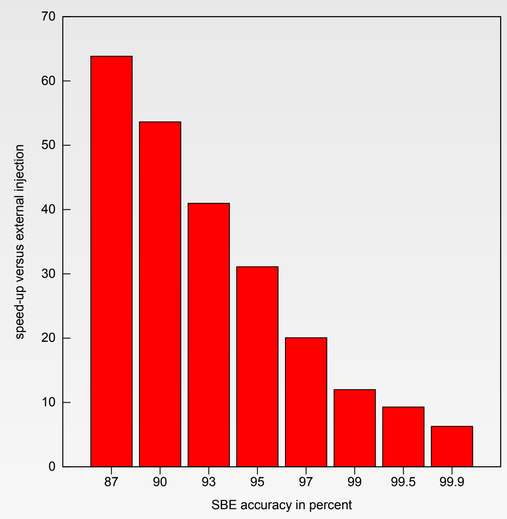
Considering the additional emulation time of redundancy different different μ result in the shortest SBE emulation time.

Optimal voting (device)



Different device sizes and by this relative SEU controller sizes do not impact significantly the optimal voting strategy.

Speed-up VS external



The achievable speed-up of the SBE flow versus external injecting depends strongly on the required SBE accuracy.

Future Work

There are two major categories:

- Execution of the SBE test flow
- Improvements to the SEU controller

References

[1] U. Kretzschmar, A. Astarloa, J. Lazaro, U. Bidarte and J. Jimenez. Robustness Analysis of Different AES Implementations on SRAM Based FPGAs. In 2011 International Conference on Reconfigurable Computing and FPGAs (ReConFig).

[2] Ken Chapman and Les Jones. SEU Strategies for Virtex-5 Devices. In *Xilinx Documentation XAPP864, http://www.xilinx.com*

[3] Xilinx Corp. Device reliability report, fourth quarter 2010. In *Xilinx Documentation UG116, http://www.xilinx.com*