# Design and Implementation of Fault-tolerant Soft Processors on FPGAs

System Level Integration Group, School of Engineering, University of Edinburgh, Scotland, UK
Chuan Hong, Khaled Benkrid, Xabier Iturbe, Ali Ebrahim
{CHong, K.Benkrid, X.Iturbe, A.Ebrahim}@ed.ac.uk

## FPGA Embedded Processors

FPGA embedded processors have found increasing uptake in many applications due to their flexibility and close compatibility with high level applications

**Xilinx FPGA Embedded Processors:**

- Xilinx MicroBlaze
- Xilinx PicoBlaze
- IBM PowerPC 405
- ARM Cortex-A9

**Altera FPGA Embedded Processors:**

- Nios II Processor
- Intel E6xxC Processor
- ARM® Cortex-A9 MPCore, Cortex-M1
- MP32 Processor
- V1 ColdFire Processor

However, SRAM-based FPGAs, the most successful commercial FPGAs, suffer from a higher susceptibility for radiation-induced faults e.g. Single-Error Upsets (SEUs) provoked by high energy particles in space



Among all FPGA resources, the Block RAM (BRAM) is the most vulnerable component in terms of space radiation. The BRAMs used as instruction/ data memory result in ineligible threatens to FPGA imbedded processors.

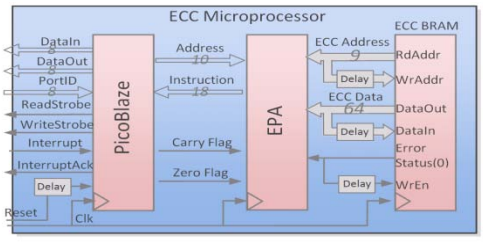
- **Spartan-3 FPGA series error rate:**
  - CLBs: 111 FIT/Mb
  - BRAMs: 222 FIT/Mb
- **Virtex-4 FPGA series error rate:**
  - CLBs: 61 FIT/Mb
  - BRAMs: 222 FIT/Mb

o *Tested at 90nm technology node*
*FIT: Failures In Time per billion hours*

## ECC Protection

The Error-Correcting Code (ECC) circuitry has been built into Xilinx FPGAs to protect BRAMs, which has the ability of:

- Single error correction
- Double error detection




**Problem:**

- Synchronization between the processor instruction fetching (commonly requires 1 clock-cycle latency) and ECC latency (2 clock-cycle latency)

**Solutions:**

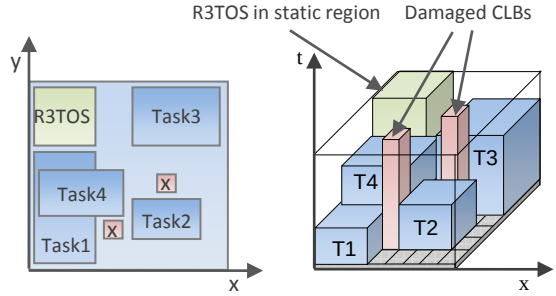
- LookAhead Algorithm: The instructions are pre-fetched in each clock cycle, and pipeline bubbles caused by branches are resolved by adding NOP operations
- ECC Processor Adaptor (EPA): the algorithm is implemented on EPA hardware mechanism. The instruction fetching is synchronized by simply connecting EPA between processor and ECC BRAM.

**Demonstration on Xilinx PicoBlaze soft-core processor:**

- Low footprint: 46 slices
- Low speed overhead: less than 10% speed loss

## Integration with R3TOS

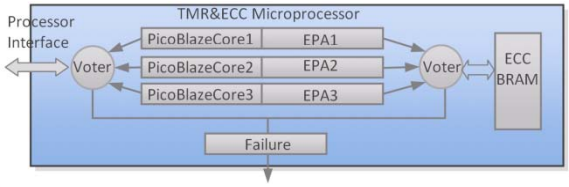
The ECC protected processor is used in the context of our Reliable, Reconfigurable, Real-time Operating System (R3TOS) to further enforce its fault tolerance.



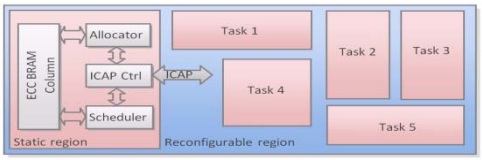

R3TOS has the ability to reconfigure hardware tasks in a time multiplexed fashion, by reusing the FPGA resources, and cater with emerging damaged resources.

## Further Fault Tolerance

The fault tolerance of the ECC protected processor is further enhanced by using Triple Modular Redundancy (TMR)




By integrating the ECC protected processors into the R3TOS, the system has the ability to autonomously recover from a Single Error Upset (SEU)




## Conclusion and Future Work

➢ A fault tolerant soft processor architecture on FPGAs, using Error-correcting Code (ECC) program memory and Triple Modular Redundancy (TMR) is presented.

➢ The architecture is implemented and tested on Virtex4 FX12 FPGA, the fault tolerance is gained by 3x using the TMR technique, with low area footprint

➢ Future work includes the porting of these techniques to other FPGA soft processors e.g. Xilinx MicroBlaze and Altera Nios.