TECHNISCHE UNIVERSITÄT DRESDEN

Chair for Embedded Systems

Department of Computer Science, Chair for Embedded Systems

TOWARDS GCC-BASED AUTOMATIC SOFT-CORE CUSTOMIZATION

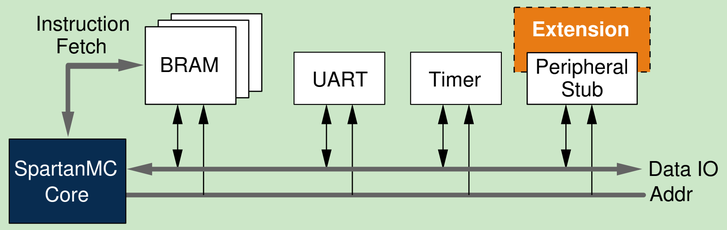
Target Architecture

SpartanMC Soft-Core Processor

- 18 bit RISC architecture tailored for FPGAs
- 3 stage pipeline
- FPGA BlockRAMs as main memory
- Sliding register window
- Memory mapped peripheral interface

Processor Extension

- Extensions implemented as memory mapped peripheral
- Interface based on static peripheral stub
  → Simple integration into current toolflow



Application Analysis

C Source Code

- Complete application sources considered for hardware extensions (even if scatted across different files)
- No code annotation required

mandelbrot.c

```
...
unsigned int in_mandelbrot_set(int x,int y) {
  ...
  while ((re_square + im_square) < 4 && (i < 200)){
     re_square = re * re;
     im_square = im * im;
     re = re_square - im_square + x
     re = 2 * re * im +y
  }
  return i;
}
...
```

main.c

```
int main() {
   ...
}
...
```

colormap.c

```
log2() {
   ...
}
...
```

Example Application

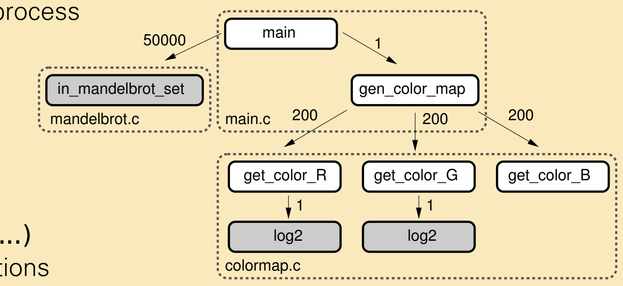
GCC Instrumentation

- GIMPLE based application analysis and modification
  → independend of input language and target architecture
- Uses GCC optimization passes for static code analysis and hardware generation
- Fully automated process
- Whole application analysis (across file boundaries) requires two consecutive GCC runs

→ **Analysis Run** and **Synthesis Run**

Analysis Results

- Generate sorted list of loop candidates from call graph
- Consider first *n* highest ranked loops (e.g. #iterations) for hardware generation process
- case *n = 1*
- reject `log2(...)`
  → 400 iterations
- select `in_mandelbrot_set(...)`
  → 50000 iterations



Example Call-Graph

Sources

1

2

Intermediate Analysis Transcript

3

3

GCC Analysis Runs

GCC Synthesis Runs

4

4

Binary Objects

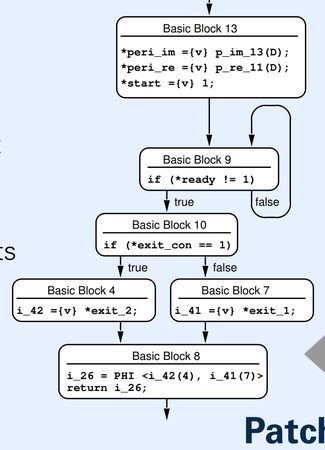
0101101
1110010
0100110
1001000
1011010

HDL Sources

HDL Generation

Generate and Adapt Binary

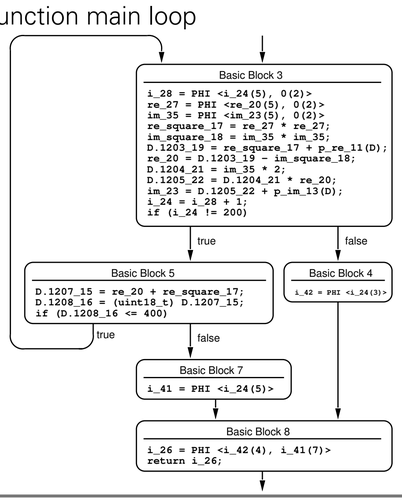
- Replace loop body in GIMPLE tree with polling loop
- Add additional Phi-Nodes for different loop exit conditions (e.g. Basic Block 10)
- Replace GIMPLE variable assignments with peripheral memory pointers



Patch GIMPLE Tree

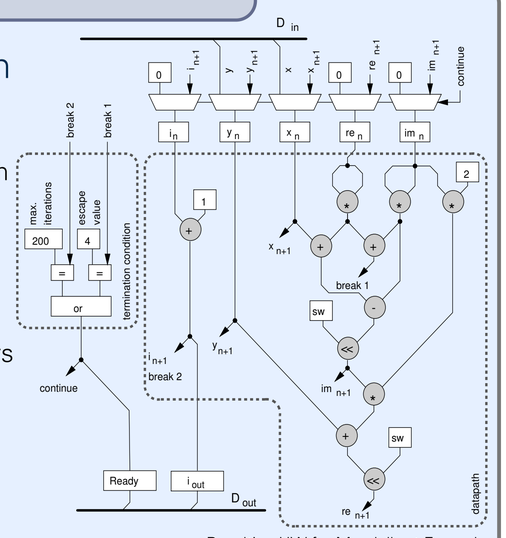
GIMPLE Tree Example

- Resulting GIMPLE tree for mandelbrot function main loop



Hardware Generation

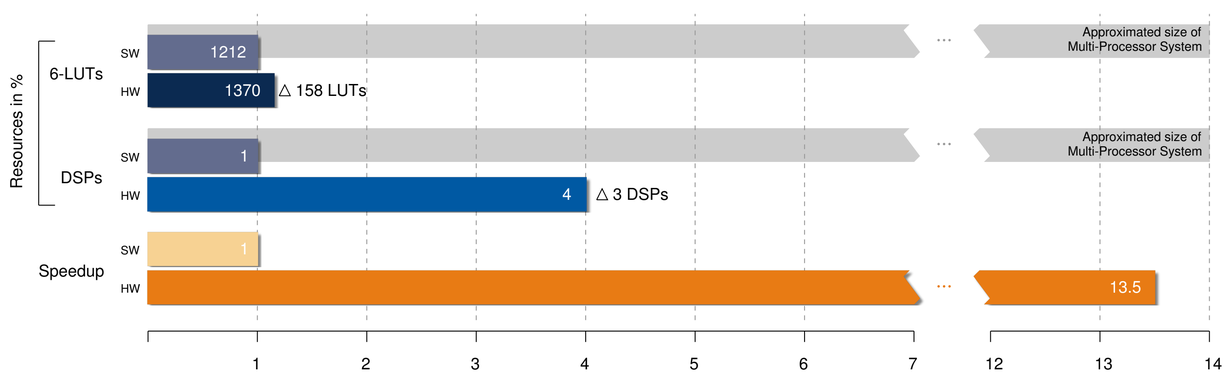
- Just as proof of concept
- Generate stateless datapath for arithmetic loop body
- Use IO registers for data transfers
- Reject code containing arrays, structures or pointers



Generate HDL Code

Resulting HW for Mandelbrot Example

Results



Resource Consumption and Speedup

- SoC contains processor, serial interface, timer and peripheral extension
- Tested on Spartan 6 (XC6sCX45T) FPGA
- Achieved a speedup of 13.5 using 158 addional LUTs and 3 DSPs

Current Restrictions and Future Work

- Only inner-most loops of functions considered for peripheral extensions
- Datapath generated as stateless net (no scheduling or pipelining) → **work in progress**
- No support for memory access (arrays, structures and pointers) → **work in progress**

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