High-Level Linear Projection Circuit Design Optimization Framework For FPGAs Under Over-Clocking

Abstract

Increase of operating clock frequency while keeping the circuit operating correctly is of extreme importance for real-time DSP. The proposed framework optimizes and mitigates the probabilistic behaviour of digital circuits, by trying to expose the impact of variability of the fabric to high-level algorithmic specifications. Circuits generated by the proposed framework outperform typical implementations of DSP applications, by minimizing area, errors, and maximizing its operating clock speed.

Linear Projection

- Karhunen-Loeve transformation
- New space: \( F = \Lambda'X \)
- Recovered space: \( X = \Lambda F + E \) (where \( E \) is the error of the approximation)
- \( Z^6 \) to \( Z^3 \) example considered

Bayesian Formulation

- The framework tries to minimize the reconstruction error:
  \[
  \min \sum \sum (AF - X)^2
  \]
- Mapping the circuit cost into a prior distribution:
  \[
  p(\Lambda) = \prod_{p=1}^{P} \prod_{k=1}^{K} p(\lambda_{pk})
  \]

Performance Evaluation

- Compared the performance:
  - Hw: proposed optimization framework
  - Ref: typical KLT implementation
  - Bayes: area optimization without information about reliability
  - Test at 510 MHz
  - 2.32 times faster than the maximum specified by the synthesis tool
  - Proposed framework:
    - Up to 39% less hardware resources.
    - Up to 8.79 dB better PSNR.

Conclusions

The proposed optimization framework optimizes a linear projection design for area, reconstruction data PSNR and resilience to operation under over-clocking simultaneously, by inserting information regarding the area and performance of the arithmetic units.

Introduction

- Smaller silicon technology has increased process variation, imposing larger guard band for operating frequencies.
- Synthesis tools are conservative and don’t know the actual device being targeted.
- The proposed framework aims to automatically generate optimal circuit designs for linear projections, taking into account the characterization of devices to operate beyond the maximum clock frequency determined for correct operation, shown as ‘Region Of Interest’.
- FPGAs were considered because they can be reconfigured. It permits to have a prior characterization of independent parts of the system on the device and later implementation of an optimized circuit on the same characterized fabric.

Optimization Framework

![Optimization Framework Diagram]

The author would like to thank Fundação para a Ciência e Tecnologia for the support through grant SFRH/BD/69587