Thermal-Aware Partitioning for 3D FPGAs

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ABSTRACT

Three-dimensional FPGA is one of the promising innovations which can lead to the reduction in delay, area and power. There is an absolute necessity to develop algorithms and software tools to exploit the advantages of the third dimension, and to solve complex tasks associated with them. Also, thermal issues are cited as critical concern in 3D integration which results in degradation of device performance. In this paper we are proposing an idea for thermal-aware partitioning targeting the power/thermal-aware EDA flow for 3D FPGAs.

INTRODUCTION

◆Though area and speed have been the main research focus on FPGA architecture and EDA to date, power is likely to be a key consideration in the design of future FPGAs especially in three-dimensional platform.
◆In spite of advantages over 2D, thermal effects are expected to be significantly higher in 3D chips due to the higher power density and this can cause greater degradation in device performance and chip reliability.
◆Additionally, excessive heat dissipation is one of the most critical challenges today. Concentration on power and thermal issues at the early stage of design cycle will reduce the burden on later stages which are already having bigger problem size.

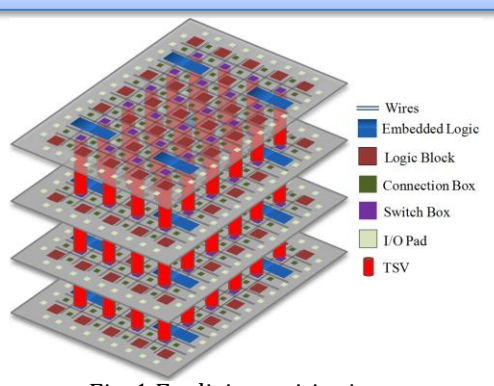

Fig. 1 Explicit partitioning

THESIS SCOPE

◆Through our research, we are proposing an EDA methodology for 3D FPGA for handling the thermal effects at the partitioning, placement and routing stages depending on the power density values as well as other effects pertaining to heat spreading, spacial and temporal effects.
◆For our target 3D EDA flow, the architecture is similar to Xilinx Virtex-II device, which is a commercial 2D FPGA, for each layer and such identical device layers are aligned vertically using through-silicon-vias (TSVs). As the TSVs handle critical signal transition between layers, their effect on thermal issues should also be considered.

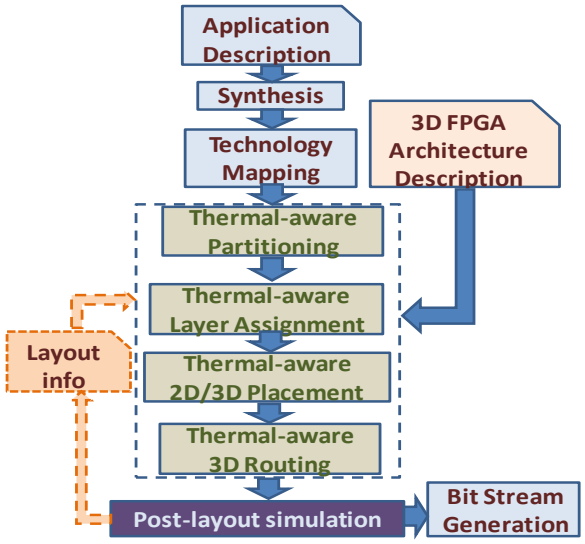

Fig. 2 Thermal-Aware 3D FPGA EDA Flow

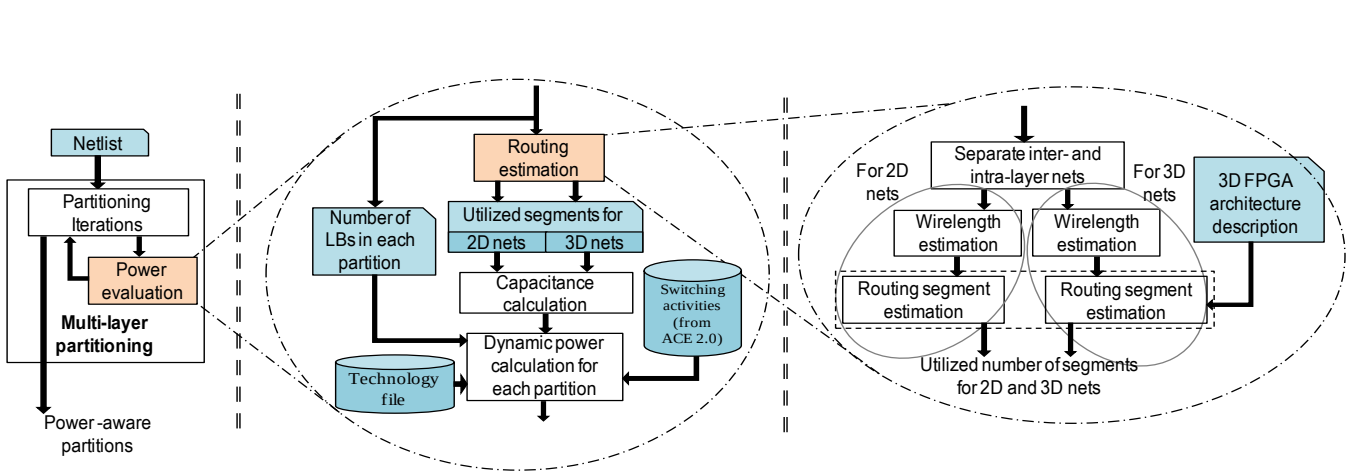

Fig. 3 (a) Power-aware partitioning algorithm (b) Power evaluation methodology (c) Hierarchical routing estimation methodology

RESULTS

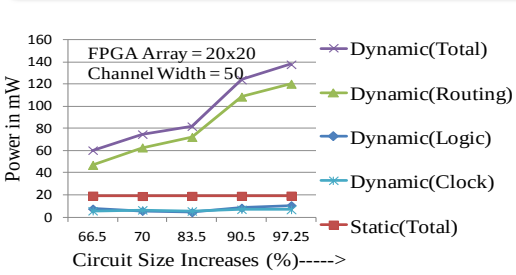

Fig.4 Power analysis for MCNC benchmark circuits on a 2D FPGA

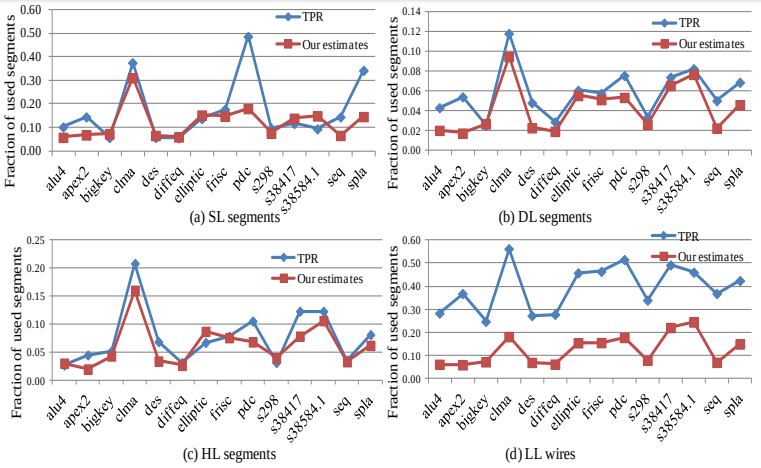

Fig.5 Estimated vs those of TPR for all four types of routing segments

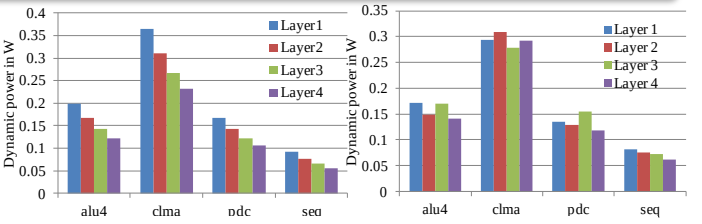

Fig. 6 Desired and Uniform Power Distribution

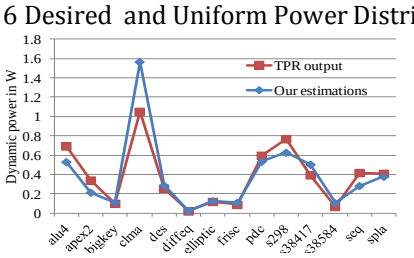

Fig.7 Estimated power values vs those of TPR

CONCLUSION

◆The implementation of the proposed work is under development. We have completed early estimation of hierarchical routing resources and power-aware partitioning for 3D FPGAs. The corresponding results have been submitted to the conferences in which our routing estimation methodology is accepted for VLSI-SoC '12 and power-aware partitioning is under review for ASPDAC'13. At present we are working on a flexible temperature model at the partitioning stage .