RECONFIGURABLE MULTI-PROCESSOR ARCHITECTURE FOR STREAMING APPLICATIONS

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INTRODUCTION

In the past decades Multi-Processor architectures have been widely utilized for the implementation of complex signal processing systems such as in the field of multimedia and wireless communications. Heterogeneous MPSoCs offer a high power efficiency and high performance but generally a limited flexibility while homogeneous architectures based on soft-cores allow a really high flexibility with the drawback of limited performance. In this context the utilization of reconfigurable hardware is exploited in order to achieve high flexibility and high computational power, expanding at the same time the range of application of the platform to different domains. The goal of reconfigurable MPSoCs is to adjust the application to the multiprocessor architecture automatically.In this paper we present a reconfigurable architecture as a processing engine for streaming applications.

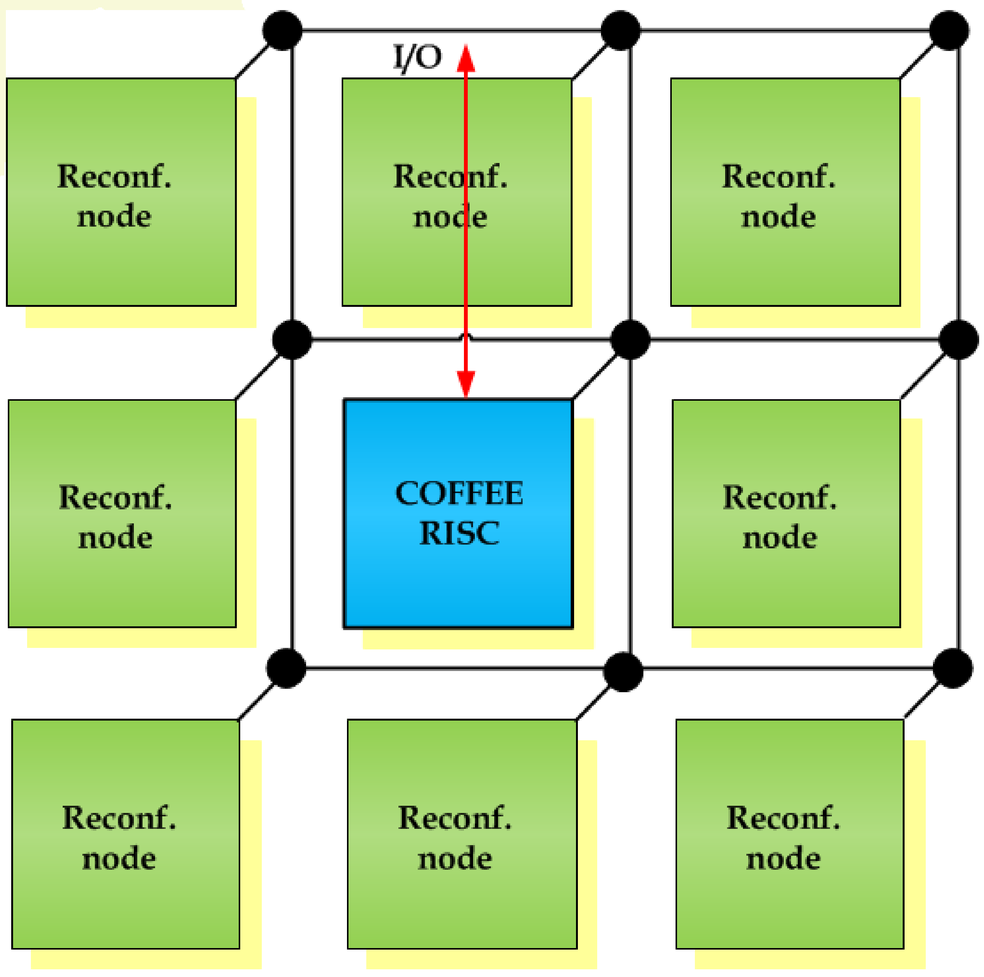

Figure 1: Overall view of the system

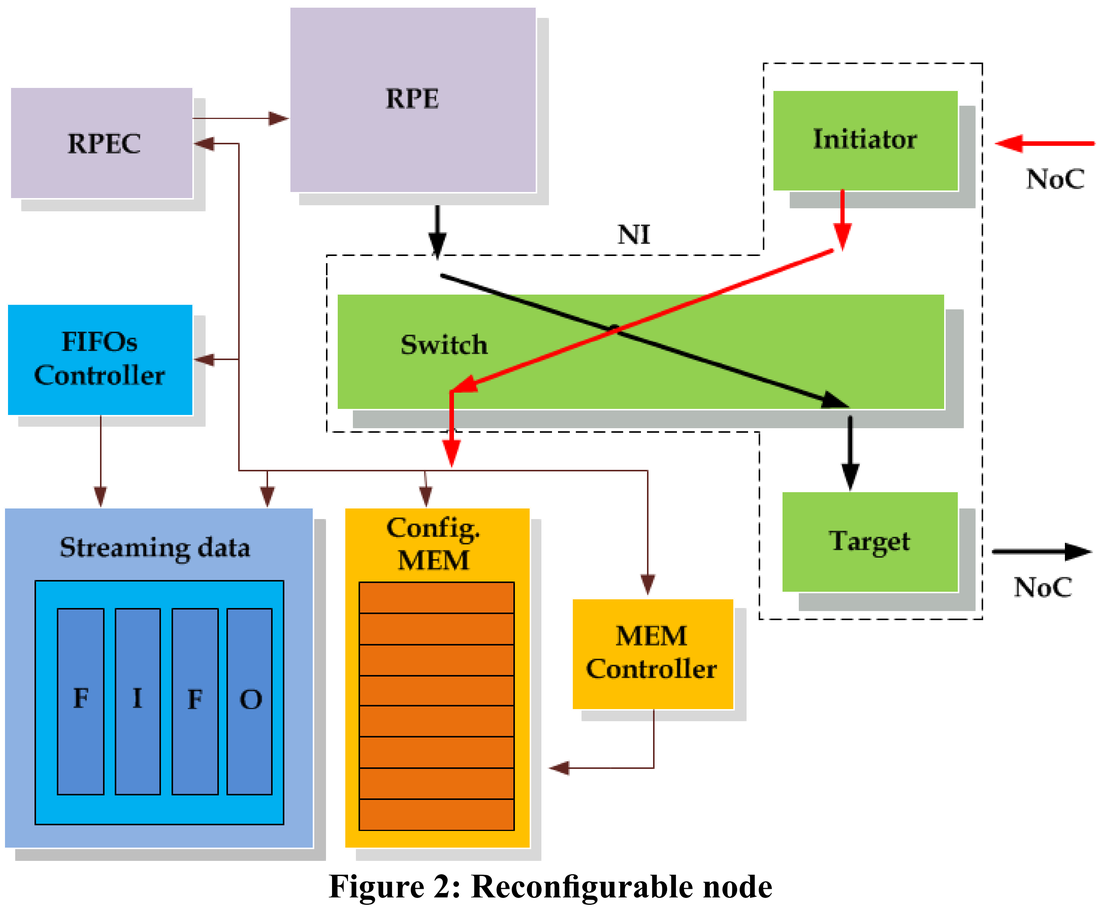

Figure 2: Reconfigurable node

ACKNOWLEDGEMENTS

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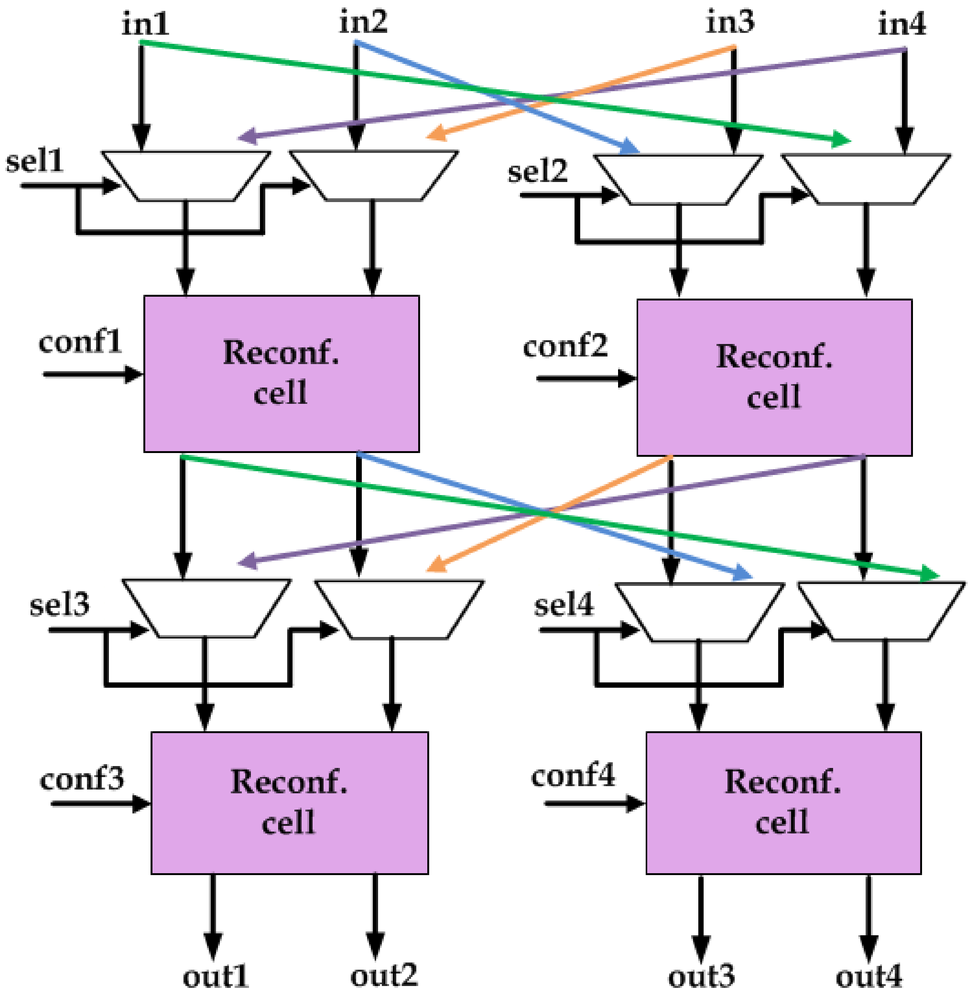

Figure 3: Reconfigurable Processing Element

RECONFIGURABLE MULTI-PROCESSOR ARCHITECTURE

Figure 1 shows the overall architecture of the system. The RISC processor acts as system controller. It is connected to the I/O, taking care of data distribution and configuration of the reconfigurable nodes at run-time. The communication between nodes is supported by Network-On-Chip (NoC). Figure 2 shows the structure of a reconfigurable node. It is composed of four main parts. The Network Interface (NI),which is composed of switch, initiator and target interfaces is responsible for data transfer to and from the NoC. Configuration Memory component stores configuration words of Reconfigurable Processing Element (RPE) and routing address of the destination node where the result stream has to be sent. Streaming data is composed of four FIFOs. When the FIFOs have been filled the data processing starts automatically and the data from the FIFOs are fed four at a time to the RPE at each clock cycle. Figure 3 shows the internal structure of the RPE, which is composed of four reconfigurable cells. The operation of each cell can be configured at run-time.

	# Registers	#Logic Elements	# DSP
System	18925	45154	144
NOC	4261	5295	0
COFFEE Node	5454	5708	16
COFFEE Core	5087	5177	16
Other peripherals	367	521	0
Reconf. Node	1143	4260	16
RPE	289	3479	16
Steaming Data	288	262	0
CONF. MEM	90	0	0

Table : FPGA synthesis results of the proposed Reconfigurable MPSOC architecture

RESULTS & CONCLUSION

This architecture architecture was simulated and synthesized on a target Stratix IV FPGA. The summary of results are shown in the Table. In this paper we have presented a work in progress reconfigurable multi-processor architecture for streaming applications. The architecture was synthesized on an Altera FPGA device and RTL simulations were carried out for the functional verification of the design. Future work will focus on the implementation of significant kernels of streaming applications to prove the validity of the proposed architecture and further hardware features will be added to the system.