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Modeling of Dynamic Reconfigurable Systems in Haskell

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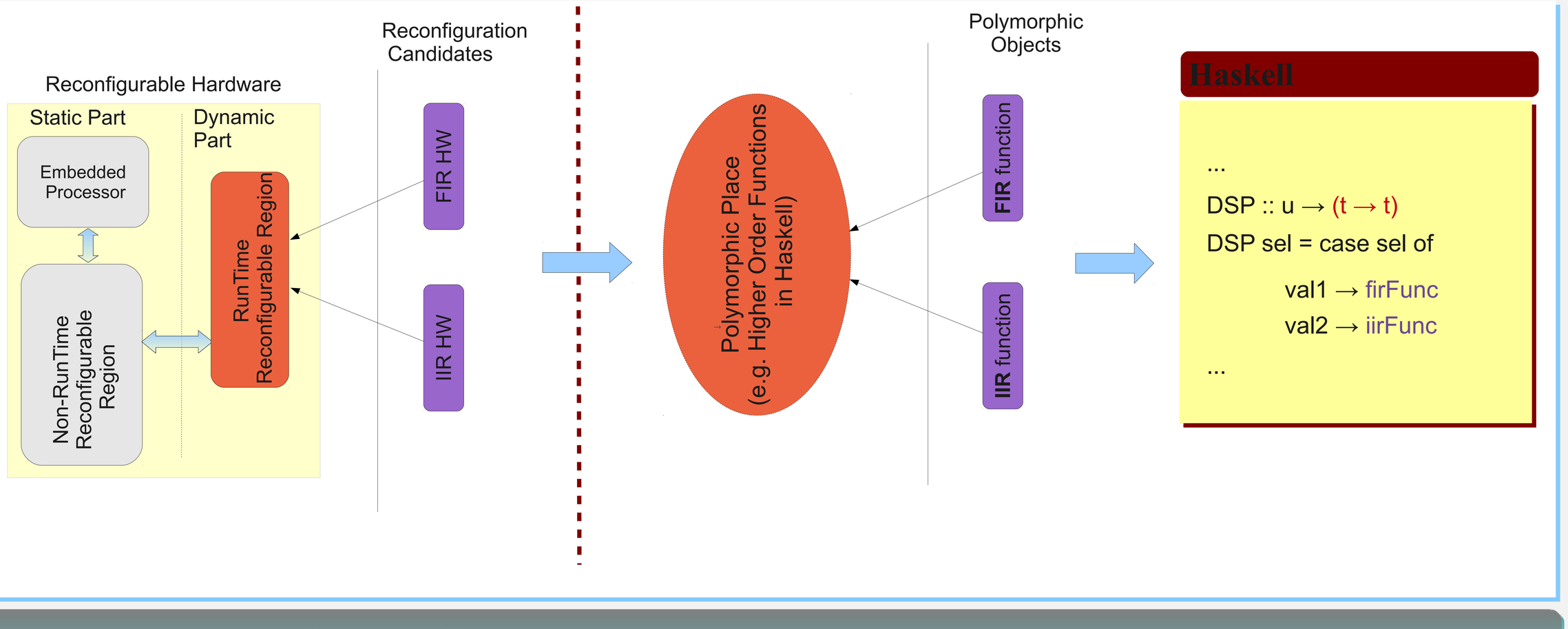
Abstract

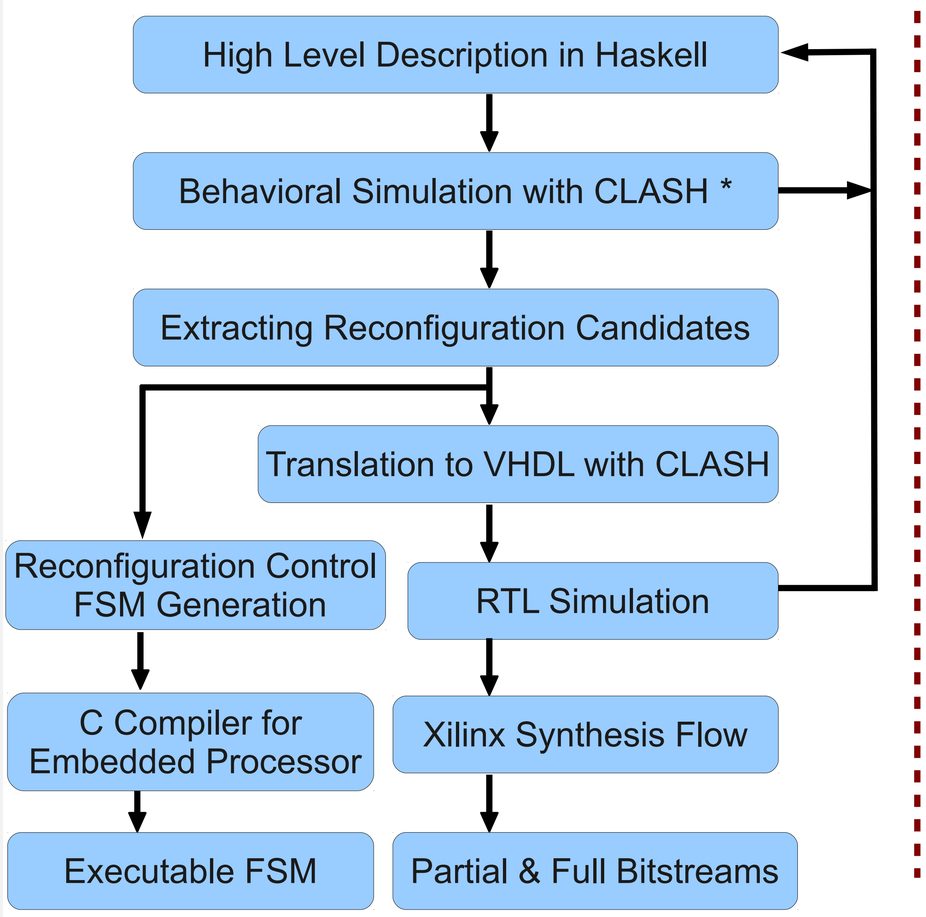
Functional HDLs can appear as an advantageous choice for formal verification and high-level descriptions. We use high-level description concepts like higher-order functions, polymorphism, parametrization, and partial evaluation to describe run-time reconfigurable systems in Haskell.

Motivation



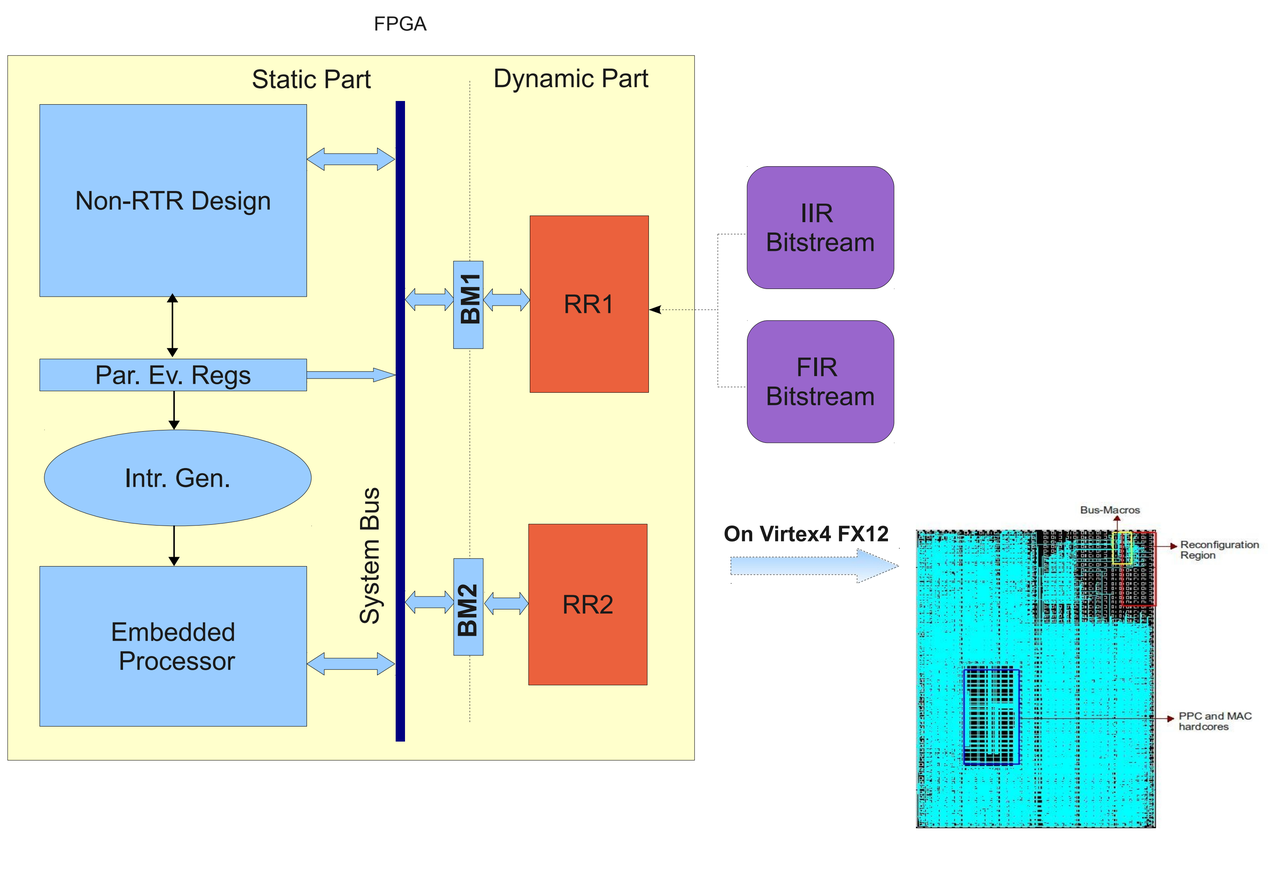
Methodology and Design Flow

Design Flow



* will include estimations for power, performance and resource usage

FPGA Implementation



Future Work and References

- **Include Timing in Models**
- **Include Formal Verification of Our Models**
- **Use More Haskell High-Level Structures Like Arrows**
- **Use Reconfiguration Combinators**
- **Include Resource Usage Estimation**
- **Include Power Estimation**

[1] Marian Adamski. Design of reconfigurable logic controllers from hierarchical UML state machines. *Electronics and Applications*, pages 82–87, May 2009.
[2] Carsten Albrecht, Thilo Pionteck, Roman Koch,Erik Maehle, and Ratzeburger Allee. Modelling Tile-Based Run-Time Reconfigurable Systems Using SystemC. ECMS2007, 4, 2007.
[3] Carlo Amicucci. SyCERS: a SystemC design exploration framework for SoC reconfigurable architecture. ERSA2006.
[4] A. Pelkonen, K. Masselos, and M. Cupak. System-level modeling of dynamically reconfigurable hardware with SystemC, *Proceedings International Parallel and Distributed Processing Symposium*, 2003.