TURNING
INTO REALITY

Architecture and FPGA Implementation of a 10.7 Gbit/s OTN Regenerator for Optical Communication Systems

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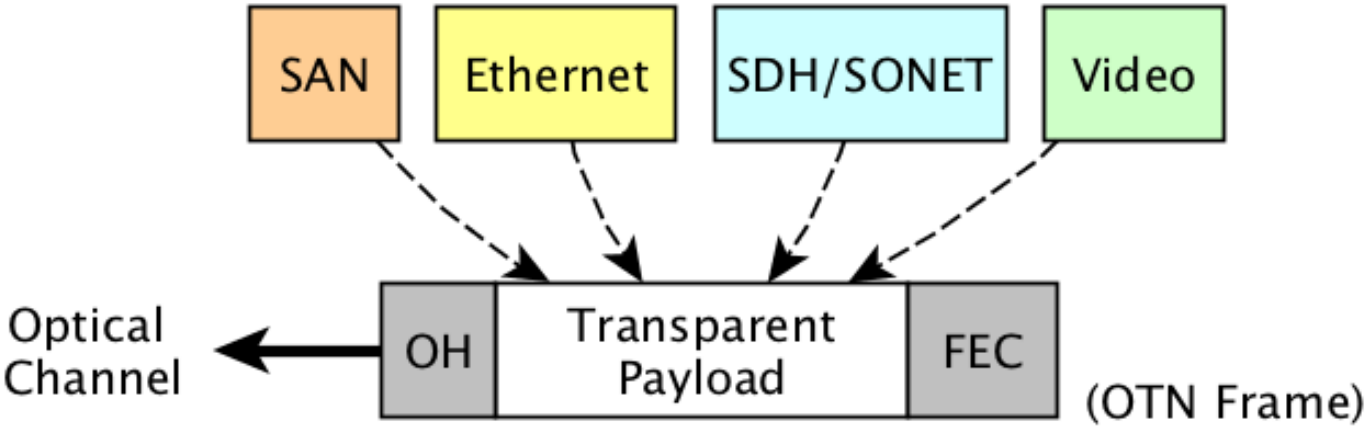
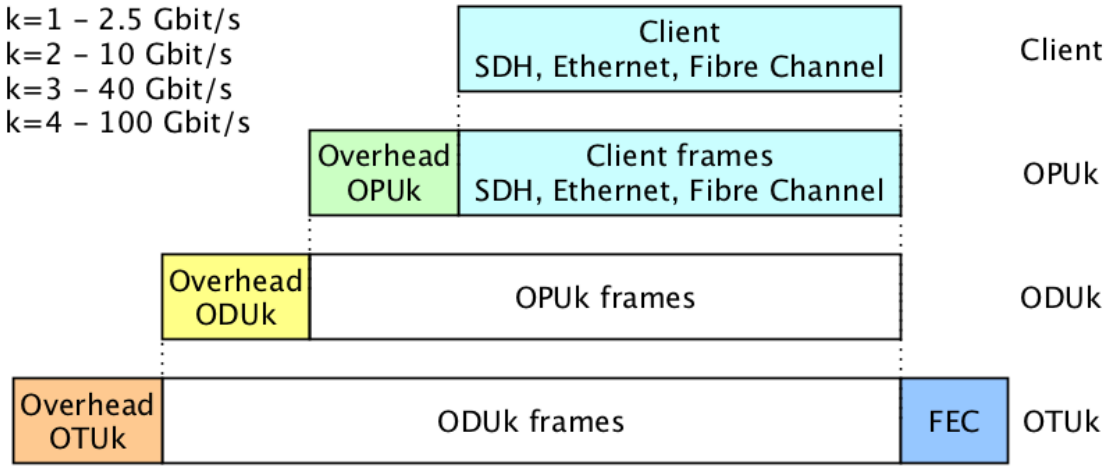
Motivation

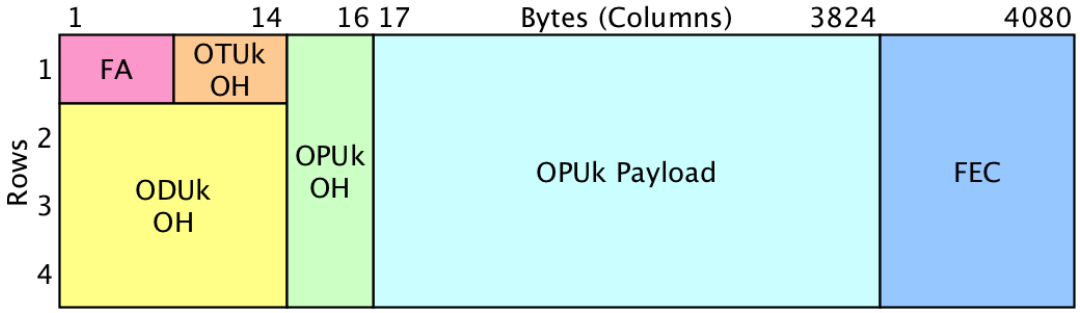
- OTN (Optical Transport Network)?
  - Refers to networks using the ITU-T G.709 standard for WDM signals
  - Provides transparent transport of different signals



Motivation

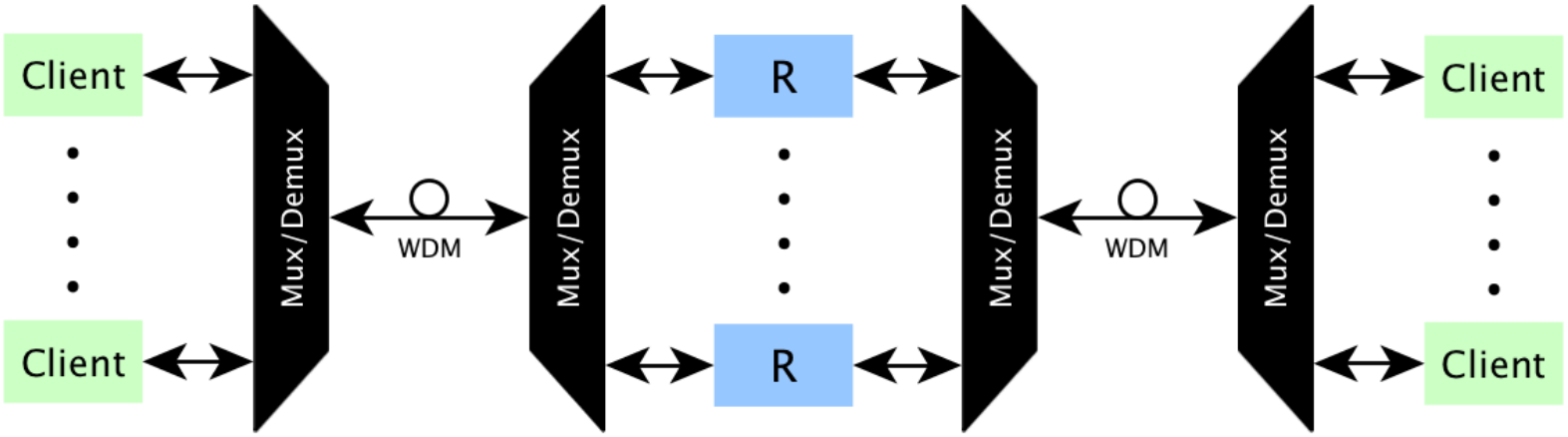
- OTN structure
  - Hierarchically organized protocol





Motivation

- Signal regeneration



Client

Encapsulated into
OTN frames

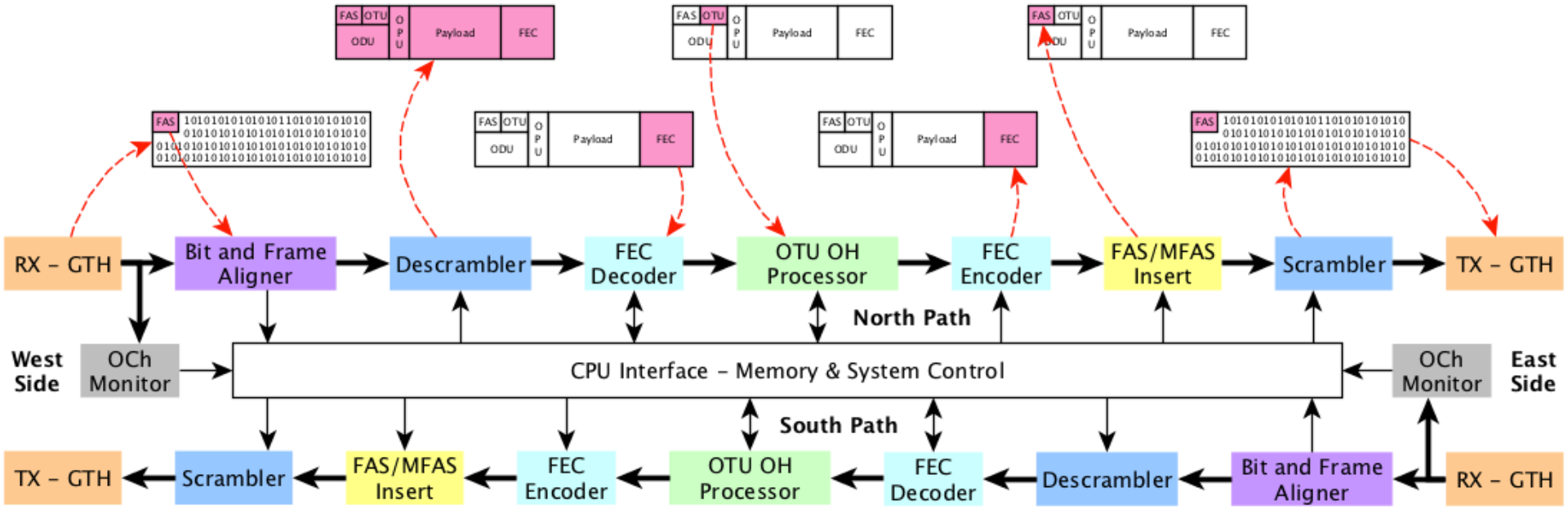
R

3R Regeneration + FEC

Re-amplification
Re-shaping
Re-timing (O/E/O)
OTU layer
FEC (error correction)

Design Architecture

- OTU2 Regenerator block diagram
  - ITU-T G.709/G.798 standards
  - Implemented in Xilinx Virtex-6 FPGA devices

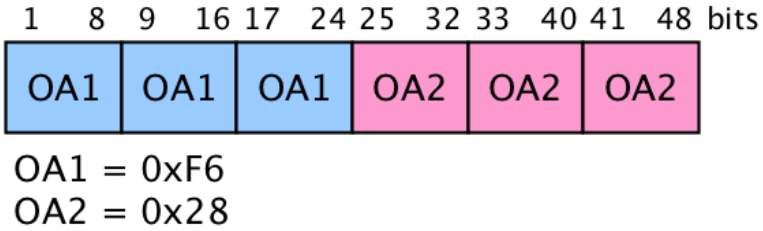


Design Architecture

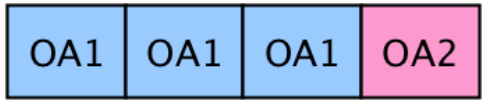
- High Speed Transceivers
  - They consist of Serializer/Deserializer devices that convert a high data rate serial signal into a parallel bus operating at lower speed
  - They provide pre-emphasis, automatic gain control, loopback test, etc…
  - In our design, the 10.7 Gbit/s OTN serial data stream (OTU2) is converted in a 64-bit bus, allowing data to be processed by the functional blocks at a much lower frequency of 167.33 MHz
  - Transceivers + Optical Modules are responsible for the 3R regeneration (O/E/O)

Design Architecture

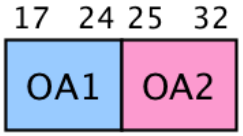
- Bit and Frame Aligner



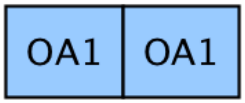
- It searches the frame alignment pattern and aligns the 64-bit data word
- 02 operation modes: **in-frame** & **out-of-frame**



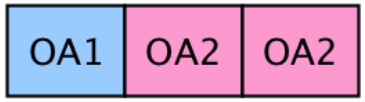
- In **out-of-frame** mode, an FSM searches the elected 4-byte sequence in two steps:



- In the first one, the transition is searched and it is aligned so that they occupy the 17th to 32nd position of the alignment pattern



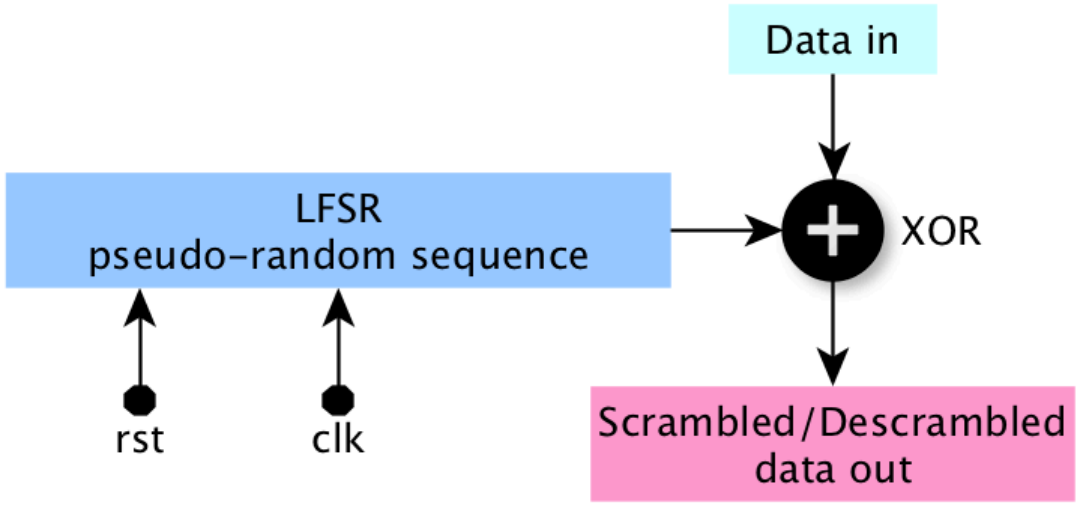
- The second step evaluates if the first two bytes of the pattern match the sequence



- In **in-frame** mode the aligner must confirm the sequence

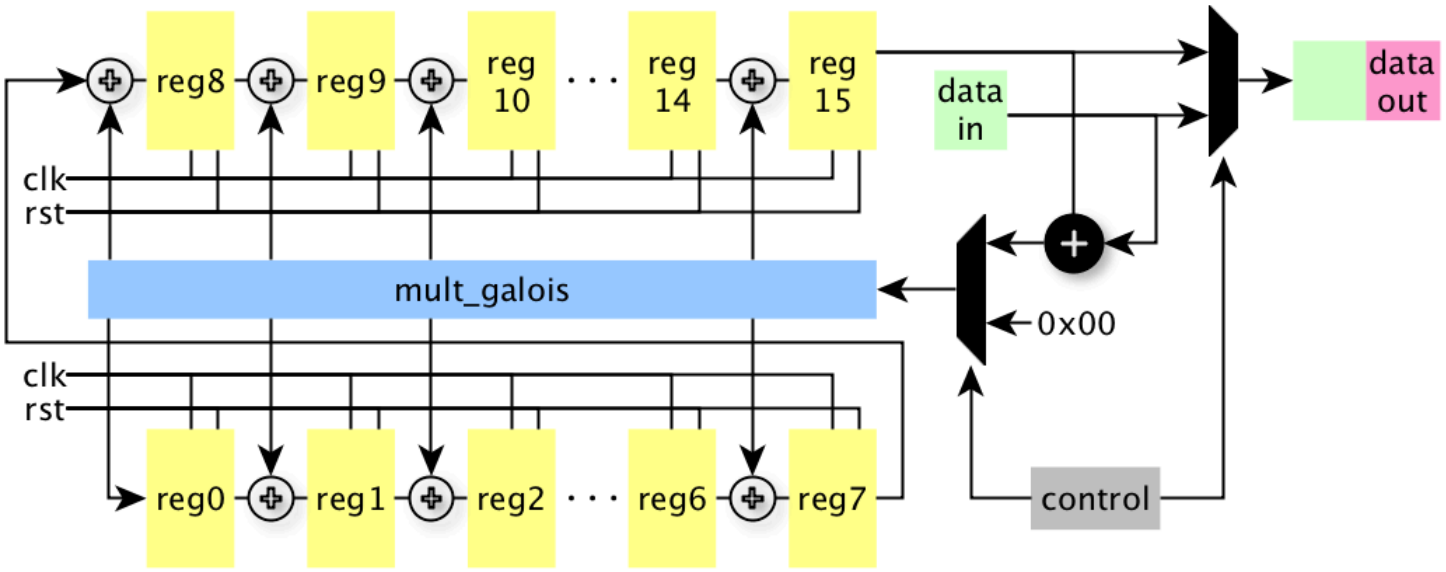
Design Architecture

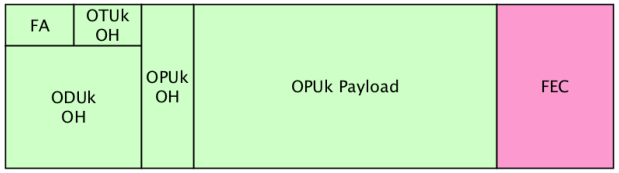
- Scrambler/Descrambler
  - Linear Feedback Shift Register circuit
  - Pseudo-random polynomial ($1 + x^1 + x^3 + x^{12} + x^{16}$) with a known sequence of 65,535 bits
  - XOR operation



Design Architecture

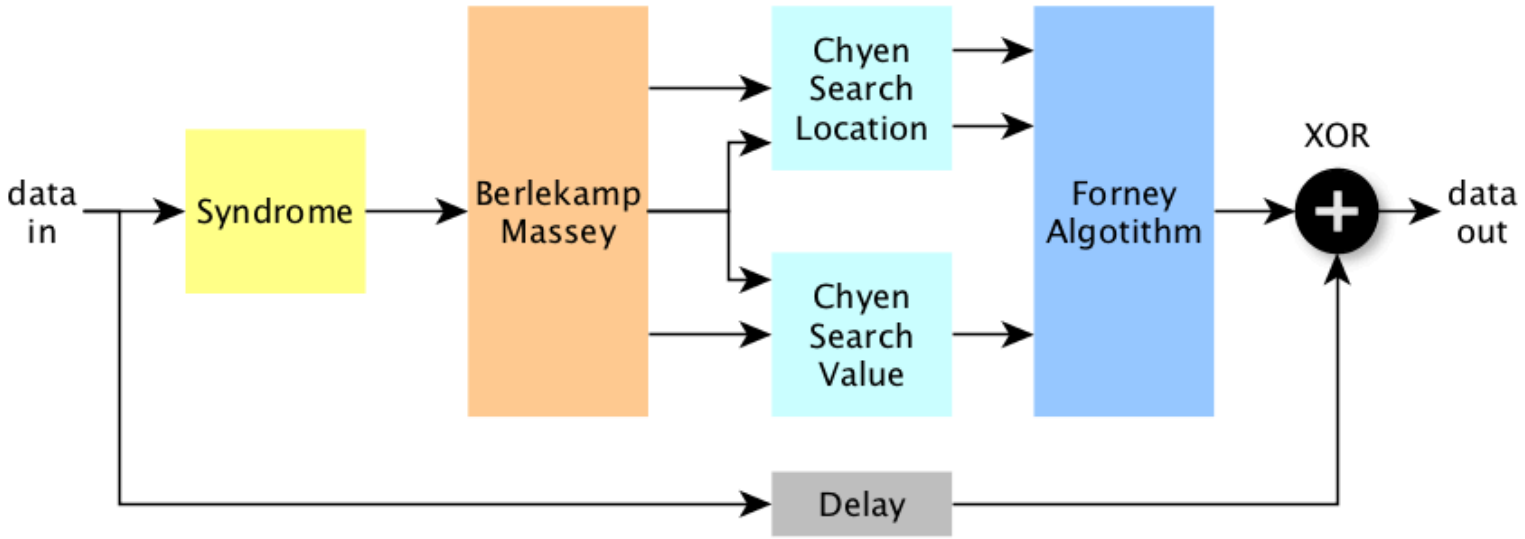
- Forward Error Correction RS(255,239)
  - The **Encoder** uses feedback shift registers for calculation and insertion of parity symbols, and also includes adders and multipliers that perform operations in accordance with the Galois algebra





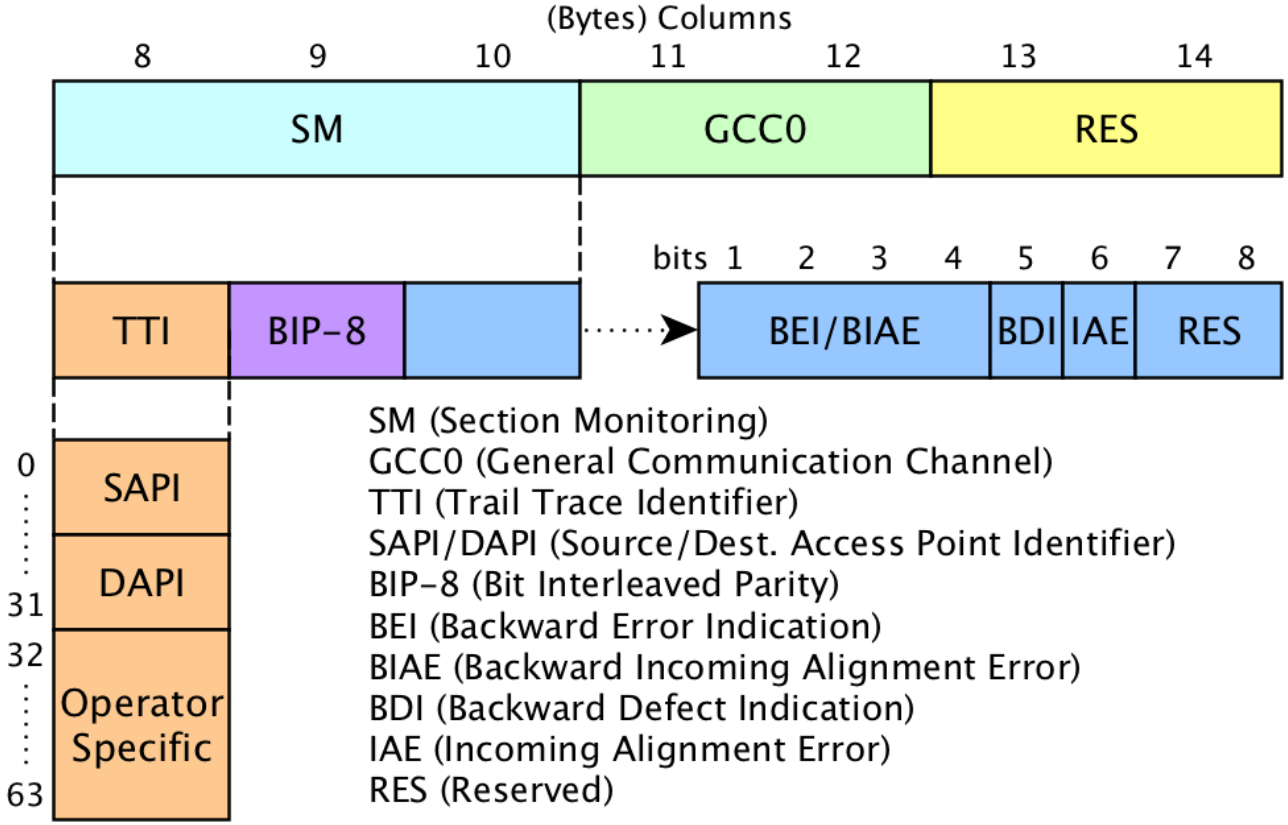
Design Architecture

- Forward Error Correction RS(255,239)
  - The **Decoder** has four functional blocks: Syndrome, Berlekamp Massey Algorithm, Chyen Search and Forney Algorithm
  - The block also provides corrected bit counters for use in statistical analysis of the transmission path



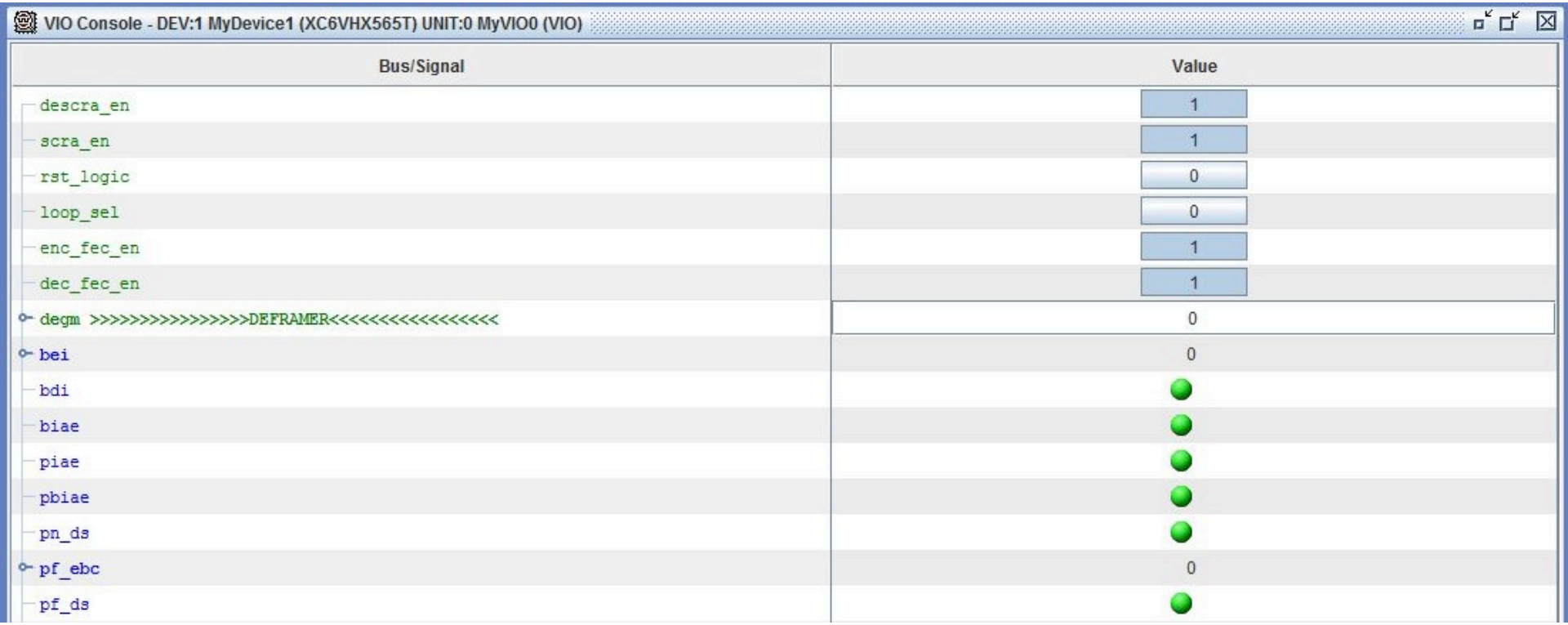
Design Architecture

- OTU OH Processor
- OTU Layer monitoring



Design Architecture

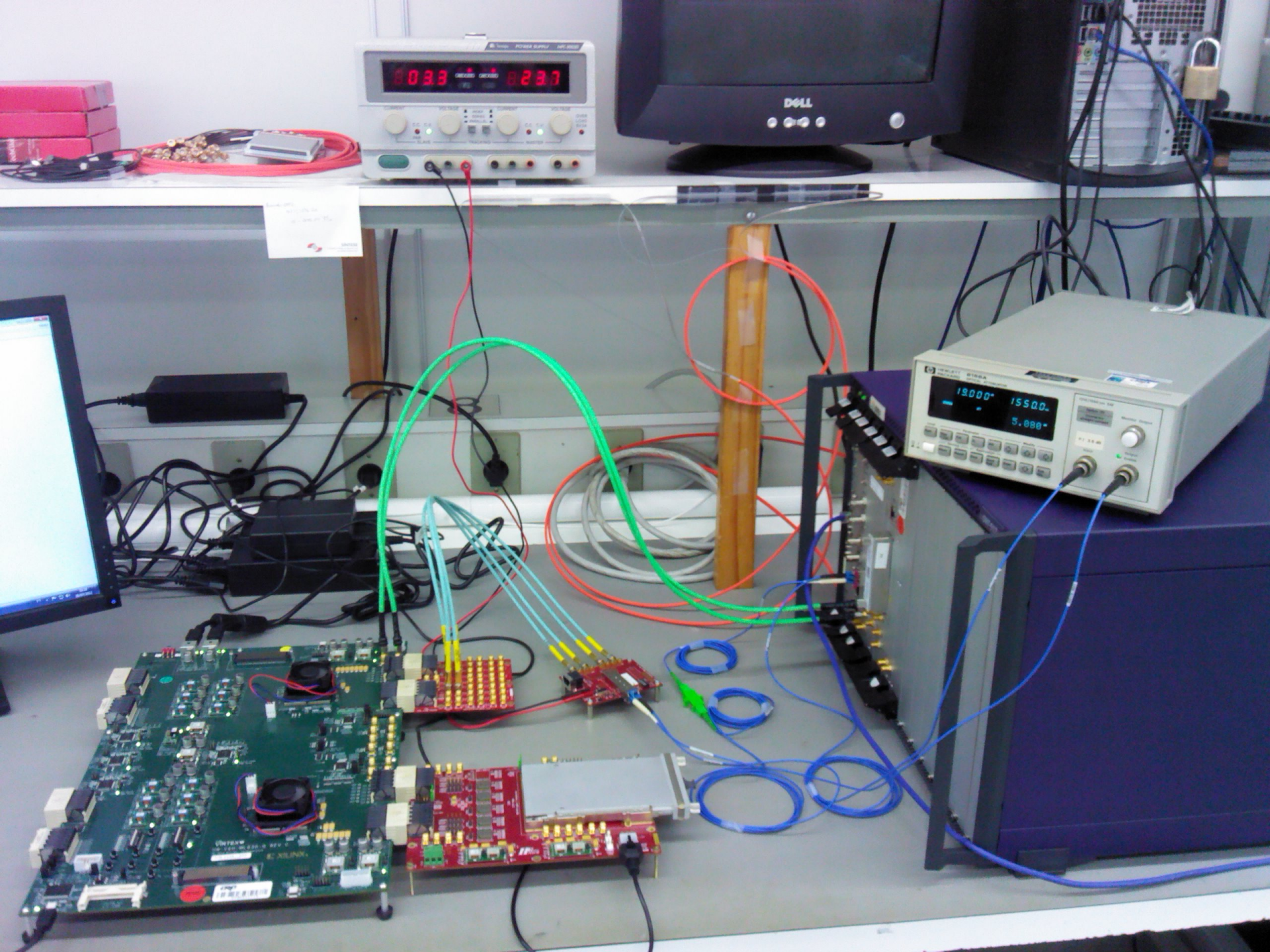
- System control
  - To emulate the CPU Interface, we have used Xilinx ChipScope as an I/O controller to manage the blocks



Design Prototyping

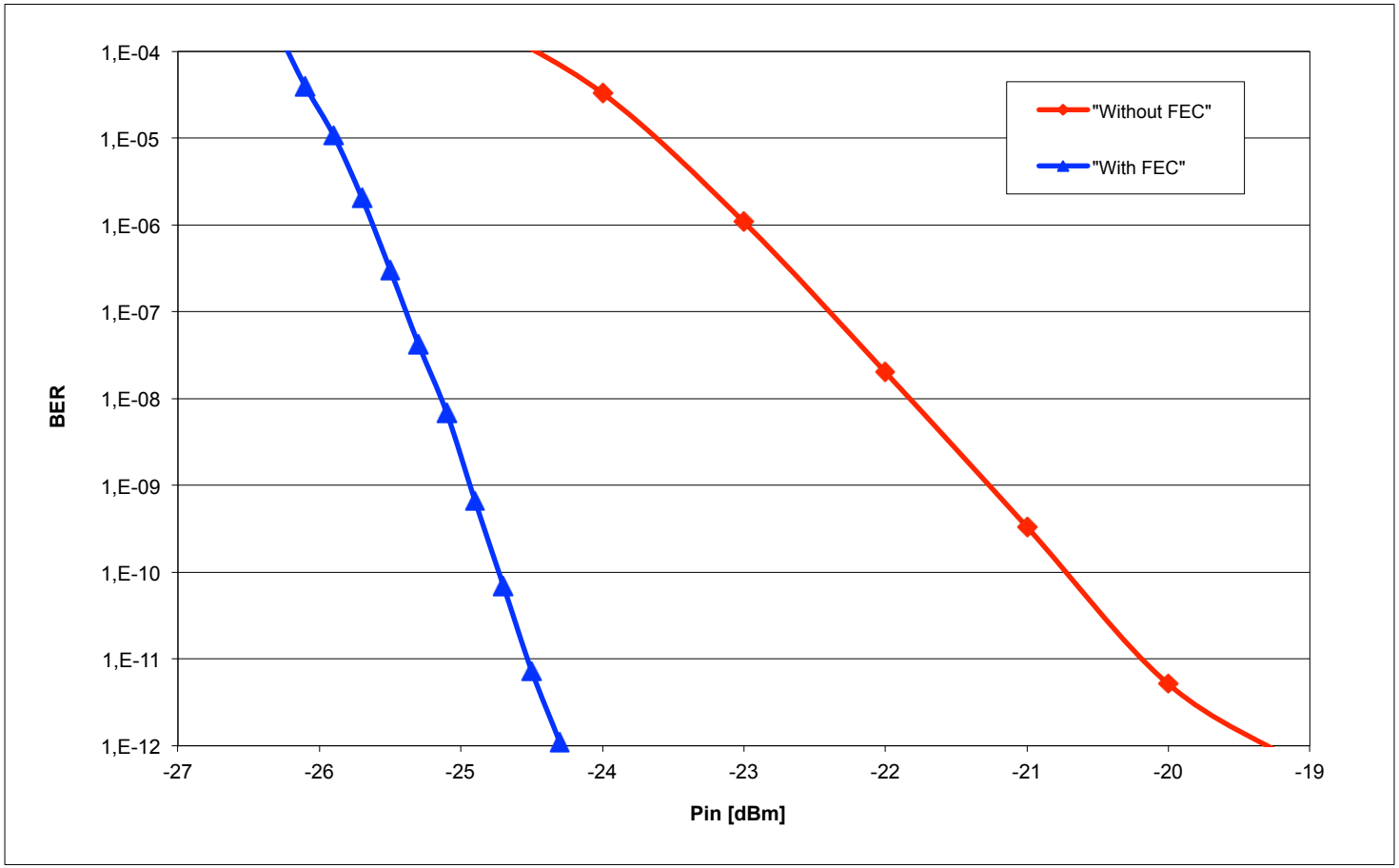
- Resource usage
  - The FEC Decoder block represents about 80% of the overall resource utilization of the complete design

Blocks	Number of Slice Registers			Number of Slice LUTs		
	Used	Available	Utilization	Used	Available	Utilization
Bit & Frame Aligner	268	708480	0.04%	892	354240	0.25%
Scrambler/ Descrambler	131		0.02%	164		0.04%
FEC Encoder	2872		0.40%	2848		0.80%
FEC Decoder	16458		2.32%	27693		7.82%
Deframer function	626		0.09%	587		0.16%
Framer function	468		0.07%	198		0.05%
FAS/MFAS Insert	65		0.01%	56		0.01%
Complete OTN Regenerator	**53869**	**708480**	**7.60%**	**81607**	**354240**	**23.04%**


DELL

Design Prototyping

- Sensibility @ 1.E-12 = **-19.60 dBm** / **-24.55 dBm** (FEC)
- Gain = **4.95 dB**



Conclusion

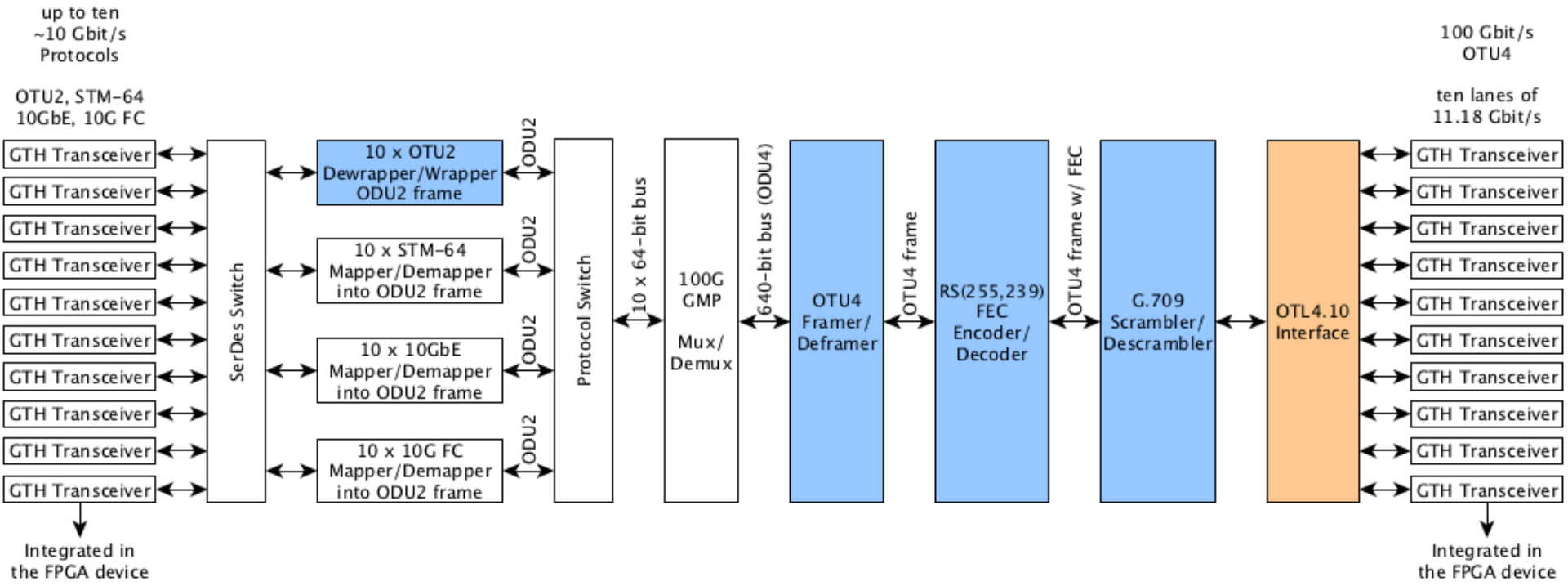
- Newest transceivers enable the implementation of high-speed telecommunication systems in a single FPGA, not requiring critical external components such as SerDes devices

- Even working with the state of the art in high operating frequency FPGAs, pipeline stages were necessary in the logic implementation to allow the timing requirements to be achieved

- Experimental results showed that the design is compliant with the standards

Ongoing Work

- 100G Muxponder
  - The colored blocks are ready



Thank You!

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