Mapping Logic to Reconfigurable FPGA Routing

Karel Heyse
Karel Bruneel and Dirk Stroobandt
Karel.Heyse@UGent.be
FPGA configuration

Programmable routing

I/O block

Logic Block

{0 0 0 1 0 1 0 0 0...}

Configuration

Ghent University – Computer Systems Lab – FPL 2012 – 30 August 2012
Parameterized Configuration

Parameters

\{ 0 \ 1 \ 0 \ A+B \ AB \ A \ 1 \}

A \quad B
\begin{align*}
0 & \quad 0 & \{0 \ 1 \ 0 \ 0 \ 0 \ 0 \ 1\} \\
0 & \quad 1 & \{0 \ 1 \ 0 \ 1 \ 0 \ 0 \ 1\} \\
1 & \quad 0 & \{0 \ 1 \ 0 \ 1 \ 0 \ 1 \ 1\} \\
1 & \quad 1 & \{0 \ 1 \ 0 \ 1 \ 1 \ 1 \ 1\}
\end{align*}

Applications

- Dynamic Circuit Specialization
  - Circuit optimization (smaller, faster, ...) using run-time reconfiguration
- Circuit Specialization
  - Hard coded settings of devices

Very fast generation of specialized configurations
What’s new in this work

Tunable LUTs (TLUT)

Static Connections
What’s new in this work

Tunable LUTs (TLUT)

Tunable Connections (TCON)

Mapping functionality to Tunable Connections (and TLUTs)
Outline

• FPGA configuration
• Applications
• What’s new in this work
• Toolflow
• Technology mapping
• Experiments
• Conclusion and Future work
Toolflow

Generic Stage
- Synthesis
- Technology mapping
- Placement
- Routing

Specialization Stage
- Parameter values
- Parameterized configuration
- Evaluate Boolean fn.
- Specialized configuration

Parameterized HDL design
entity multiplexer is
port(
  --BEGIN PARAM
  sel : in  std_logic_vector(1 downto 0);
  --END PARAM
  in : in  std_logic_vector(3 downto 0);
  out : out std_logic
);
end multiplexer;

architecture behavior of multiplexer is
begin
  out <= in(conv_integer(sel));
end behavior;
Toolflow

Parameterized HDL design → Synthesis → Technology mapping → Placement → Routing → Parameterized configuration
Toolflow

Parameterized HDL design → Synthesis → Technology mapping → Placement → Routing → Parameterized configuration

Tunable Connection (TCON)

TLUT & TCON network
**Toolflow**

Parameterized HDL design → Synthesis → Technology mapping → Placement → Routing → Parameterized configuration

2 Tunable Connections

- $p$
- $\neg p$
Toolflow

Parameterized HDL design → Synthesis → Technology mapping → Placement → Routing → Parameterized configuration

2 Tunable Connections
Toolflow

Parameterized HDL design → Synthesis → Technology mapping → Placement → Routing → Parameterized configuration

2 Tunable Connections
Technology mapping
Algorithm

• Minimal depth mapping

1. Cone enumeration: Finding all feasible cones per node
2. Cone ranking: Selecting best feasible cone per node
3. Cone selection: Selecting cones that provide covering
Feasibility: LUT

Cone with 3 input nodes
= LUT-feasible (3 input LUT)
Feasibility: TLUT

Cone with 3 input nodes that aren’t parameters
= TLUT-feasible (3 input LUT)
Feasibility: TCON

Equivalent to multiplexer controlled by function of parameters
= TCON-feasible
TLC supergate

One TLUT with TCONs attached to its inputs
Feasibility: TLC supergate

Equivalent to multiplexer controlled by function of parameters and LUTs at its inputs = TLC-feasible
Feasibility calculation

Based on cone function: $\Psi$

$\Psi(l_1,l_2,l_3,l_4,p,q)$
Feasibility calculation

Using Binary Decision Diagram of cone function
Feasibility calculation

Using Binary Decision Diagram of cone

ψ

f(p,q)

k(l₁,l₂,l₄)  m(l₁,l₂,l₃)  n(l₁,l₃,l₅)
Feasibility calculation

Using Binary Decision Diagram of cone

\[ \psi \]

\[ f(p, q) \]

\[ s(I_1) \]
\[ t(I_2) \]
\[ v(I_3) \]
EXPERIMENTAL RESULTS
Area and depth

Area (#LUTs)

Depth (#LUTs)
TLC supergate

Area (#LUTs)

Depth (#LUTs)

With vs. without TLC

regex 1x  regex 2x  regex 4x  tlc2  tlc4

With vs. without TLC

regex 1x  regex 2x  regex 4x  tlc2  tlc4
Execution time and scaling behaviour

Execution time

- TLUTMAP
- TCONMAP w/o TLC
- TCONMAP w. TLC

Ghent University – Computer Systems Lab – FPL 2012 – 30 August 2012
Conclusion

- Automatically map functionality to reconfigurable routing
- Creates **smaller** and **faster** mapping results
- Part of new toolflow to quickly create specialized configurations
Mapping Logic to Reconfigurable FPGA Routing

Karel Heyse
Karel Bruneel and Dirk Stroobandt
Karel.Heyse@UGent.be
Acknowledgement

- Supported by European Commission FP7 project:

- The author is supported by a Ph.D. grant of the FWO-Vlaanderen