Mapping Logic to Reconfigurable FPGA Routing

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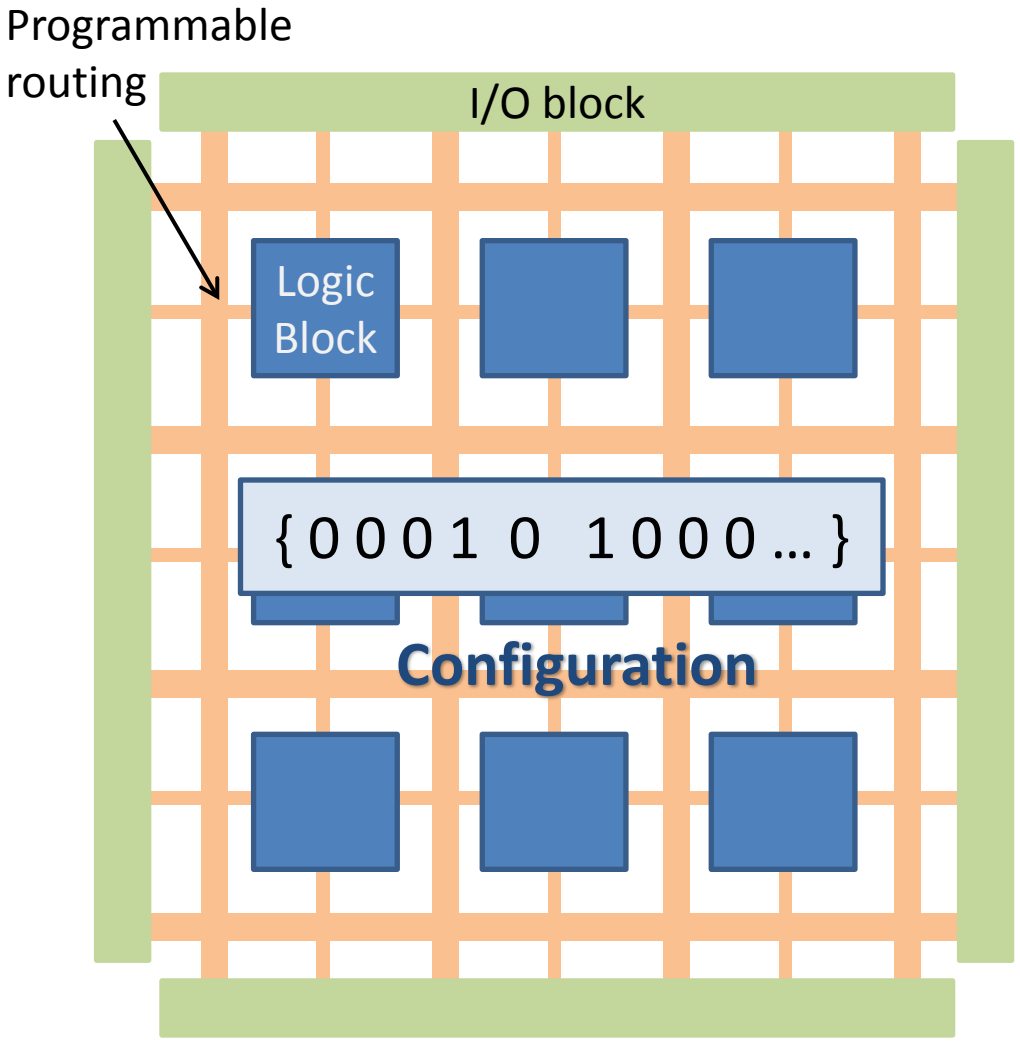
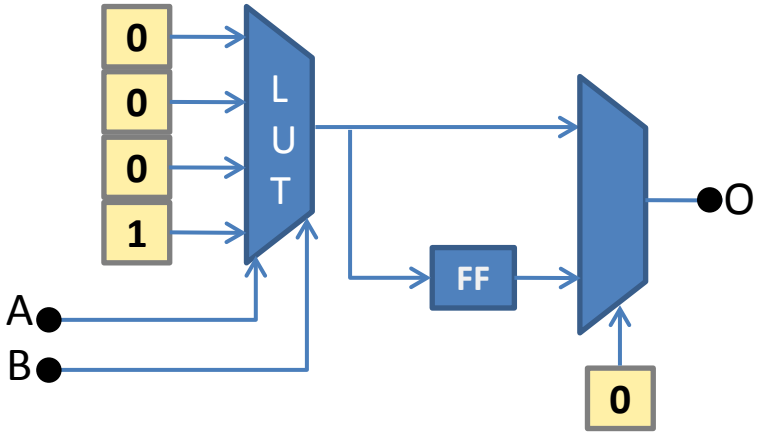
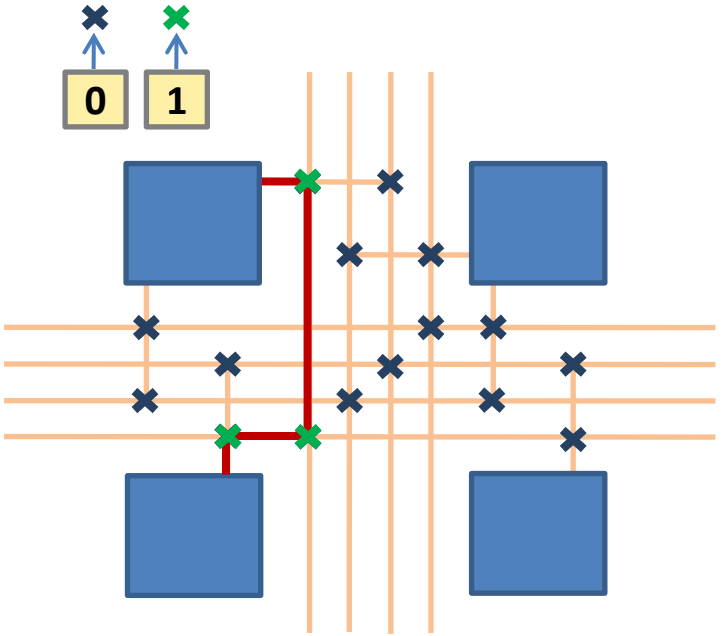
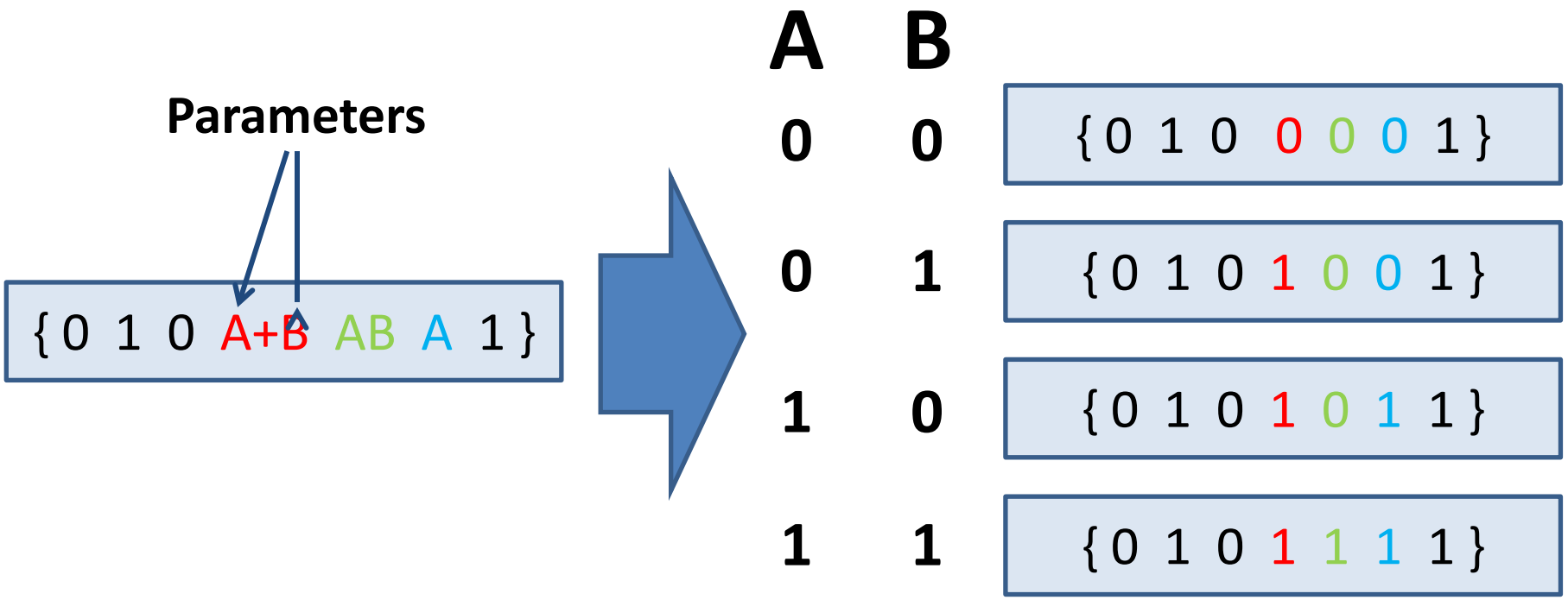
FPGA configuration







Parameterized Configuration



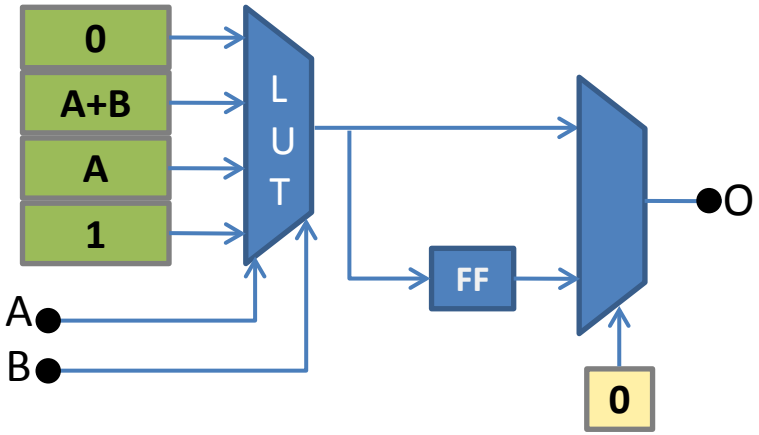
* K. Bruneel and D. Stroobandt, "Automatic Generation of Run-time Parameterizable Configurations," FPL 2008.

Applications

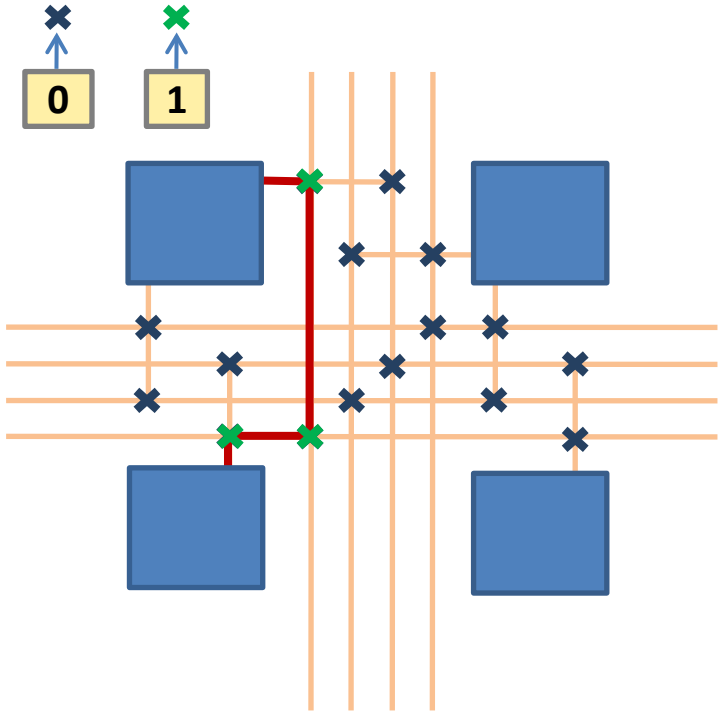
- Dynamic Circuit Specialization
  - Circuit optimization (smaller, faster, …) using run-time reconfiguration
- Circuit Specialization
  - Hard coded settings of devices

Very fast generation of specialized configurations

What's new in this work

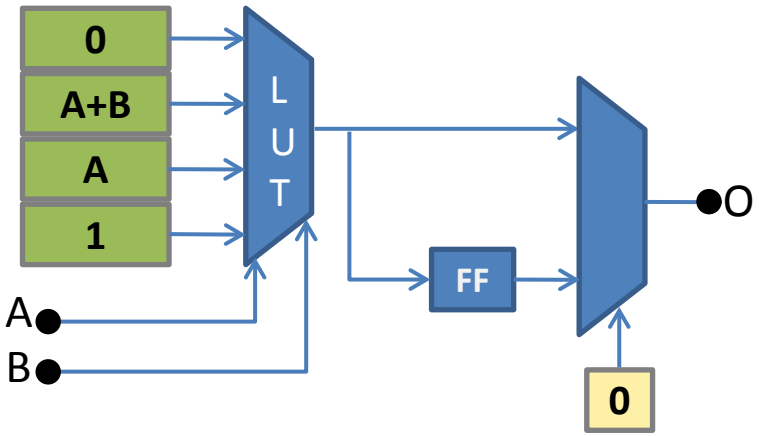


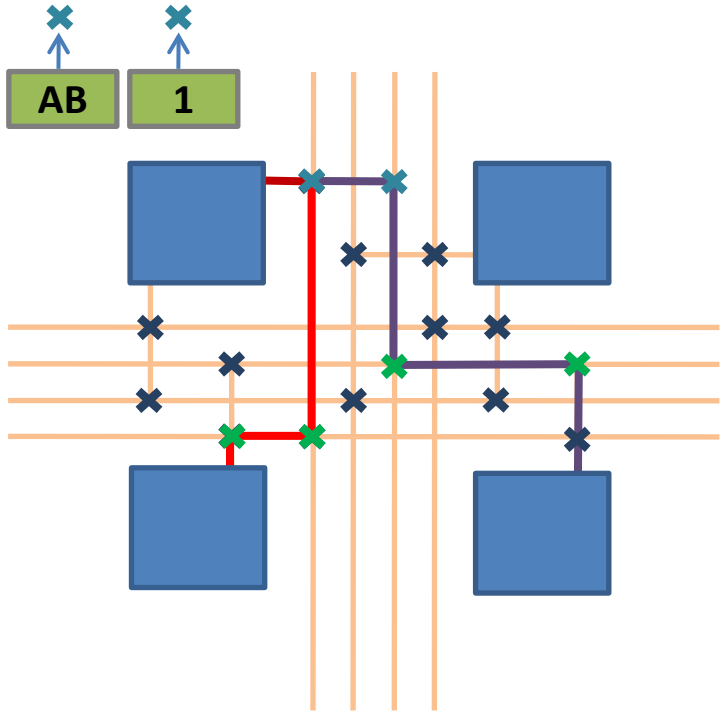
Tunable LUTs **(TLUT)**



Static Connections

What's new in this work





Tunable LUTs **(TLUT)**

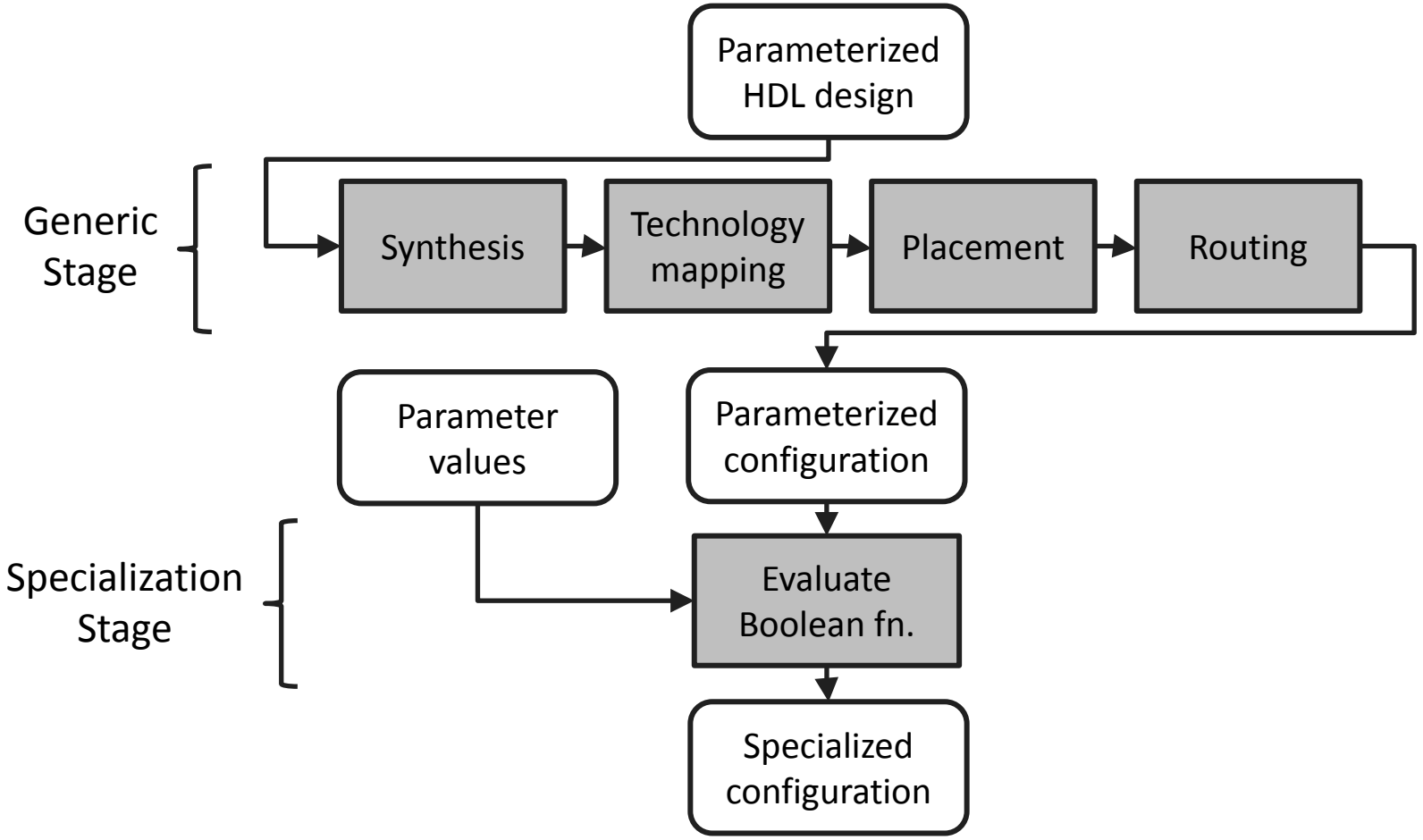
Tunable Connections (**TCON**)

Mapping functionality to Tunable Connections (and TLUTs)

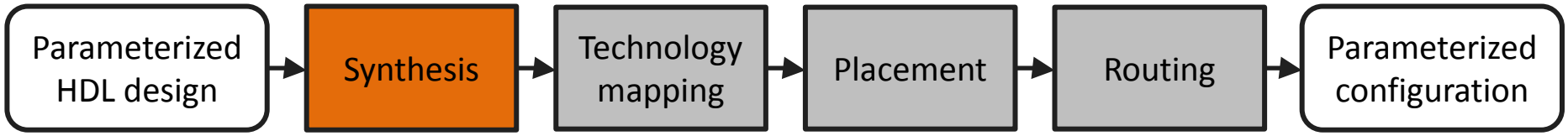
Outline

- FPGA configuration
- Applications
- What's new in this work
- Toolflow
- Technology mapping
- Experiments
- Conclusion and Future work

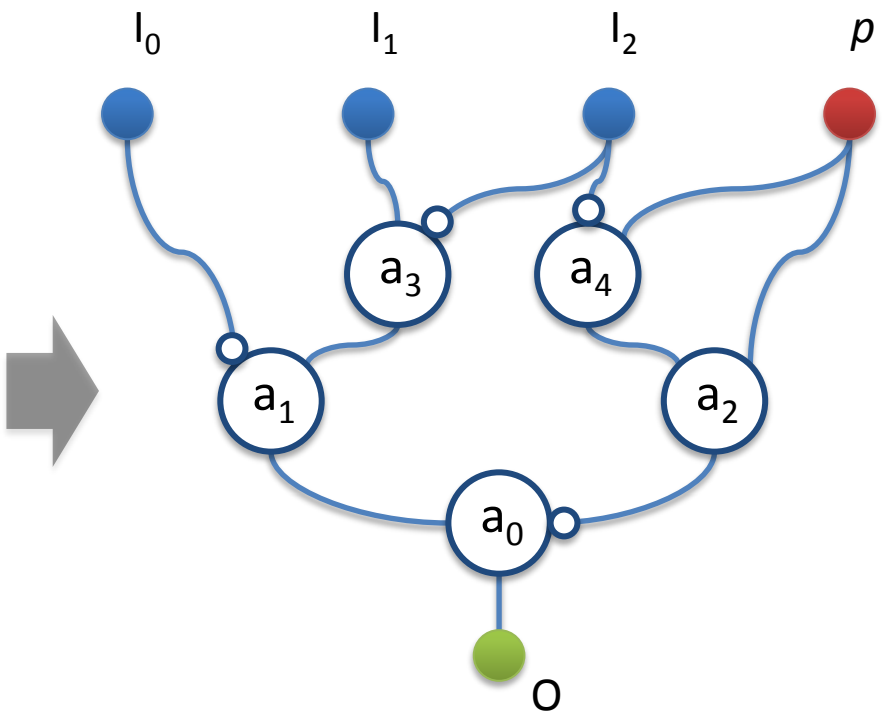
Toolflow


Parameterized HDL design
Generic Stage
Synthesis
Technology mapping
Placement
Routing
Parameter values
Parameterized configuration
Specialization Stage
Evaluate Boolean fn.
Specialized configuration

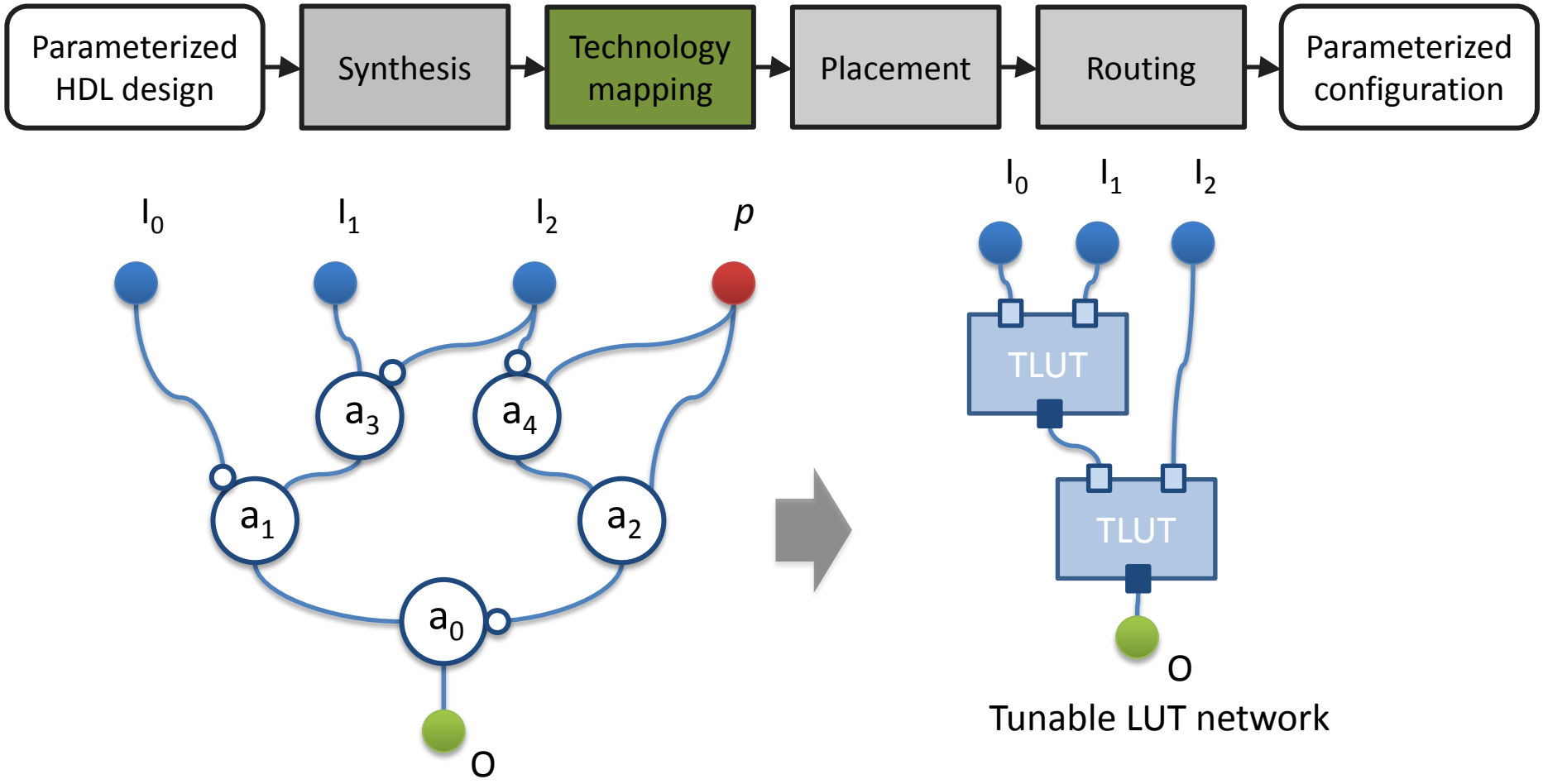
Toolflow



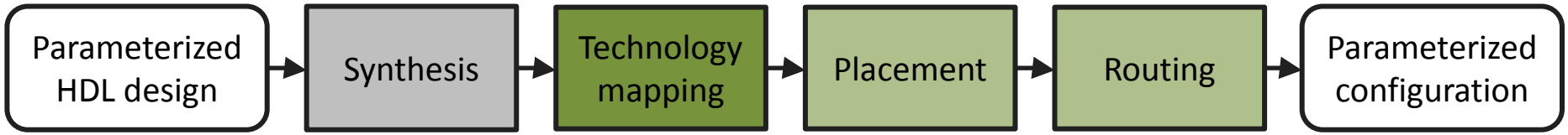

```
entity multiplexer is
port(
  --BEGIN PARAM
  sel : in  std_logic_vector(1 downto 0);
  --END PARAM
  in  : in  std_logic_vector(3 downto 0);
  out : out std_logic
);
end multiplexer;

architecture behavior of multiplexer is
begin
  out <= in(conv_integer(sel));
end behavior;
```

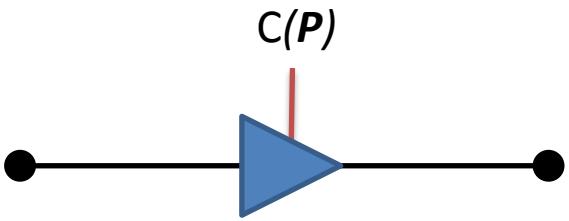


Toolflow

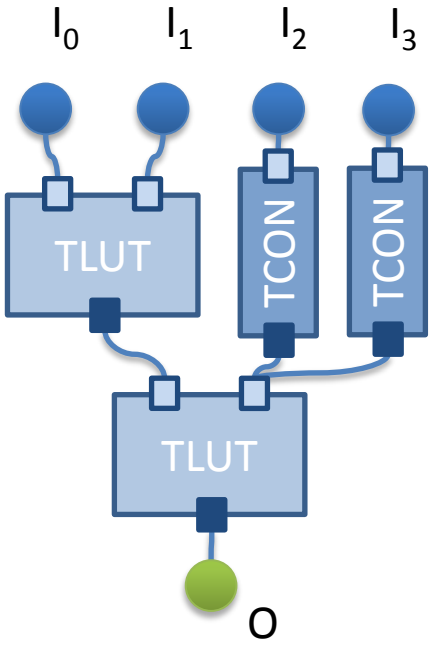

Parameterized HDL design
Synthesis
Technology mapping
Placement
Routing
Parameterized configuration
I_0
I_1
I_2
p
a_3
a_4
a_1
a_2
a_0
O
I_0
I_1
I_2
TLUT
TLUT
O
Tunable LUT network

Toolflow



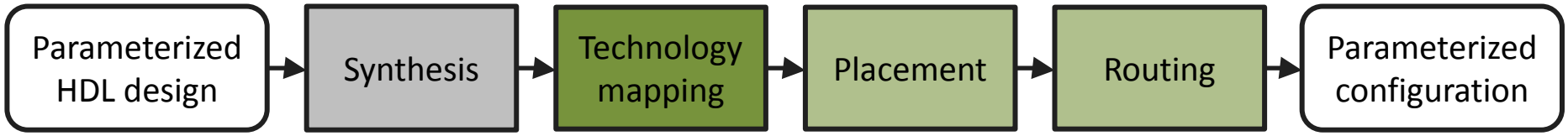


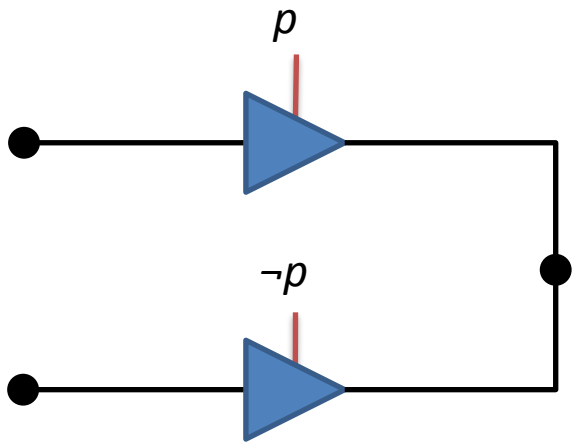
Tunable Connection **(TCON)**



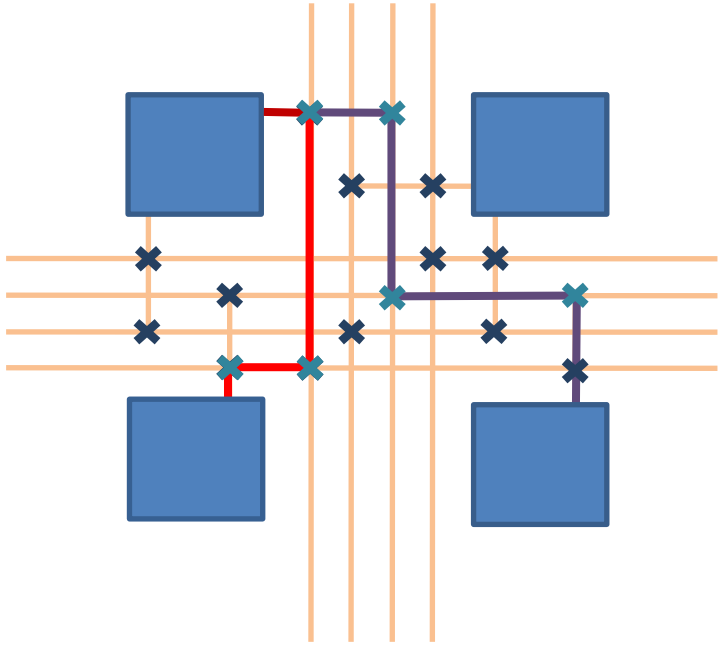
TLUT & TCON network

Toolflow

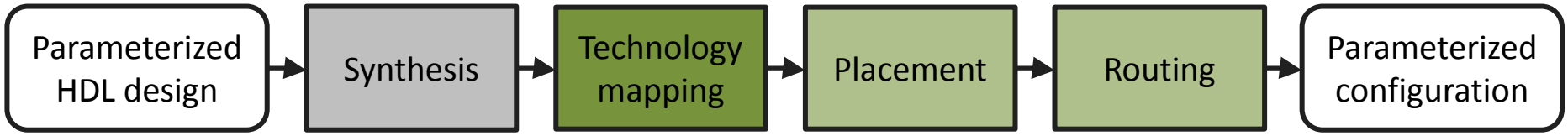


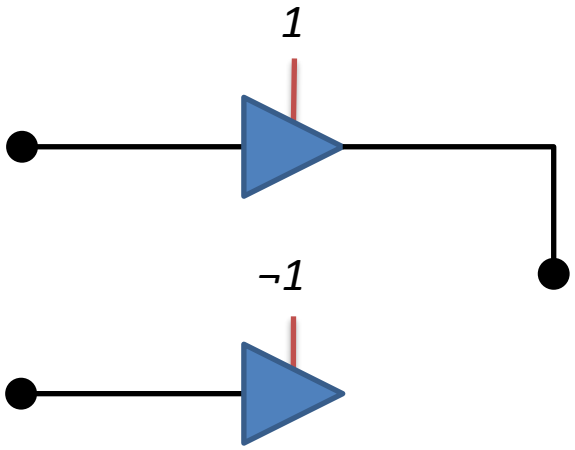


2 Tunable Connections

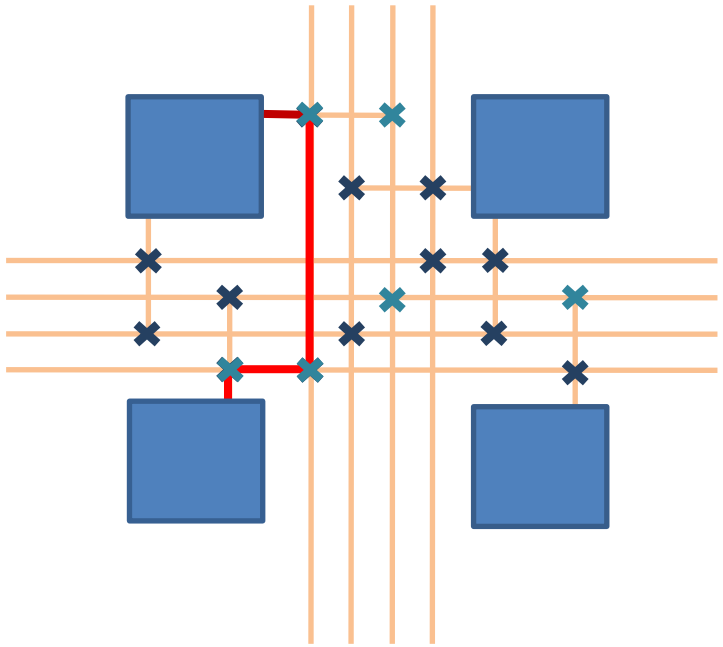


Toolflow

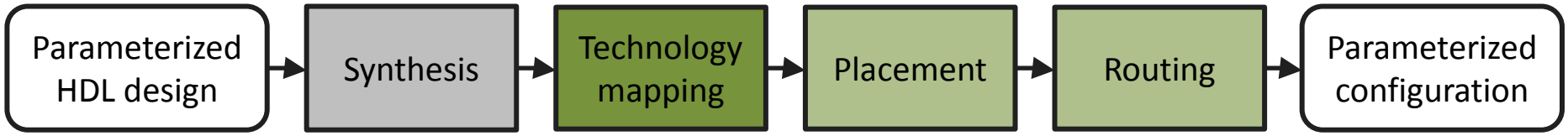


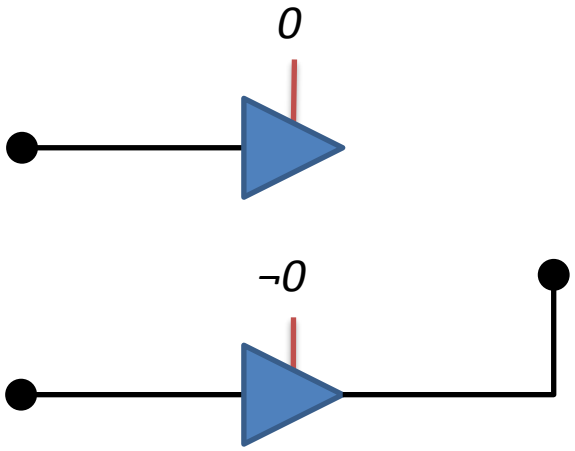


2 Tunable Connections

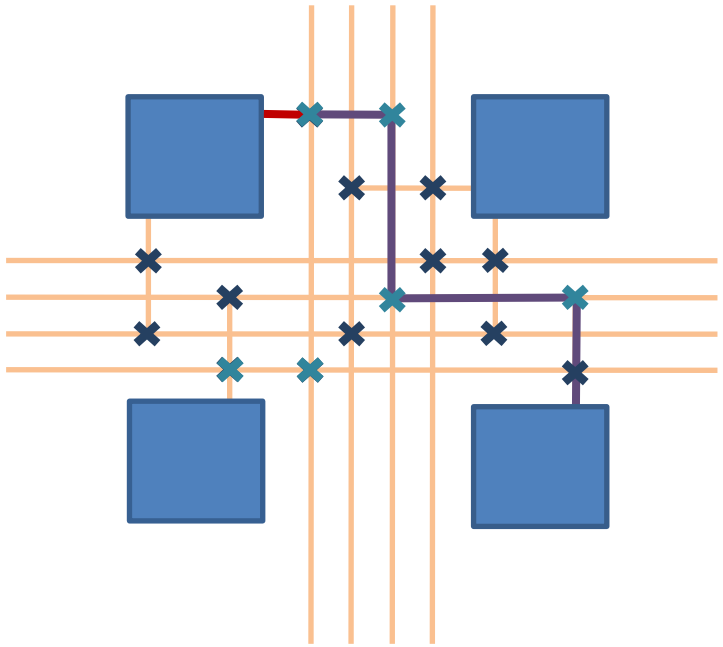


Toolflow

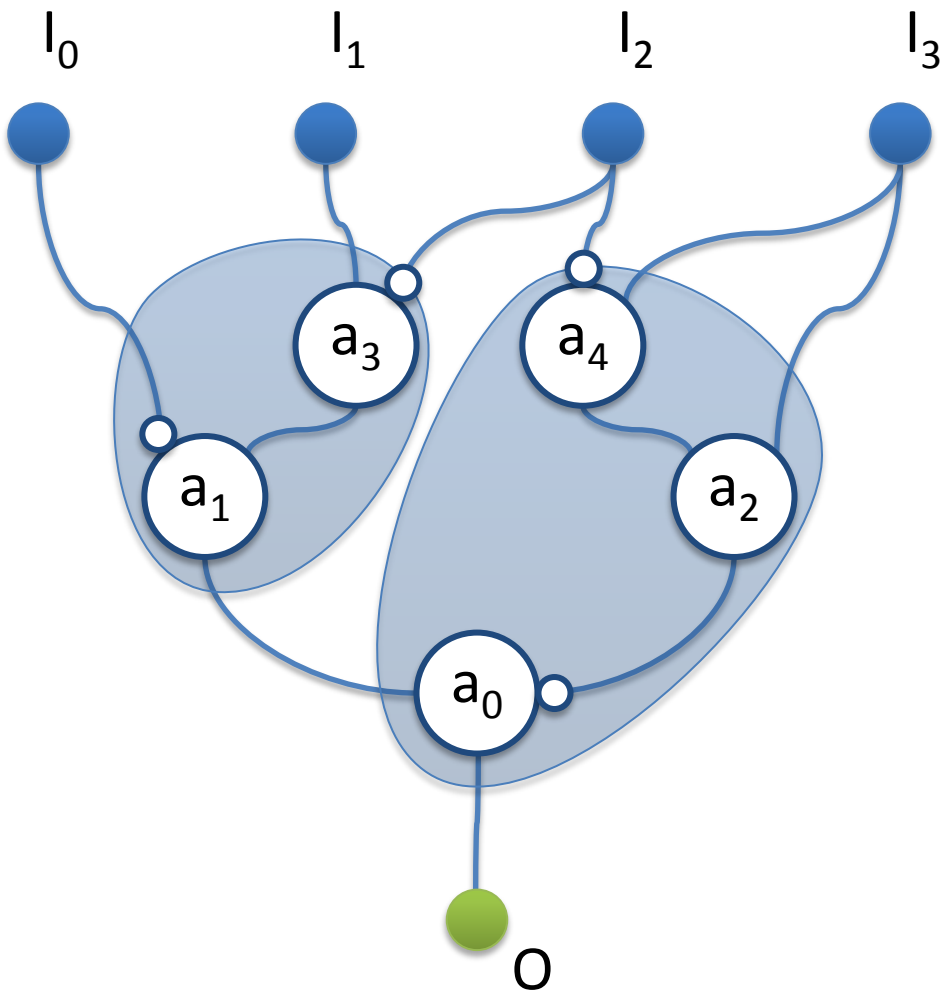




2 Tunable Connections



Technology mapping



Algorithm

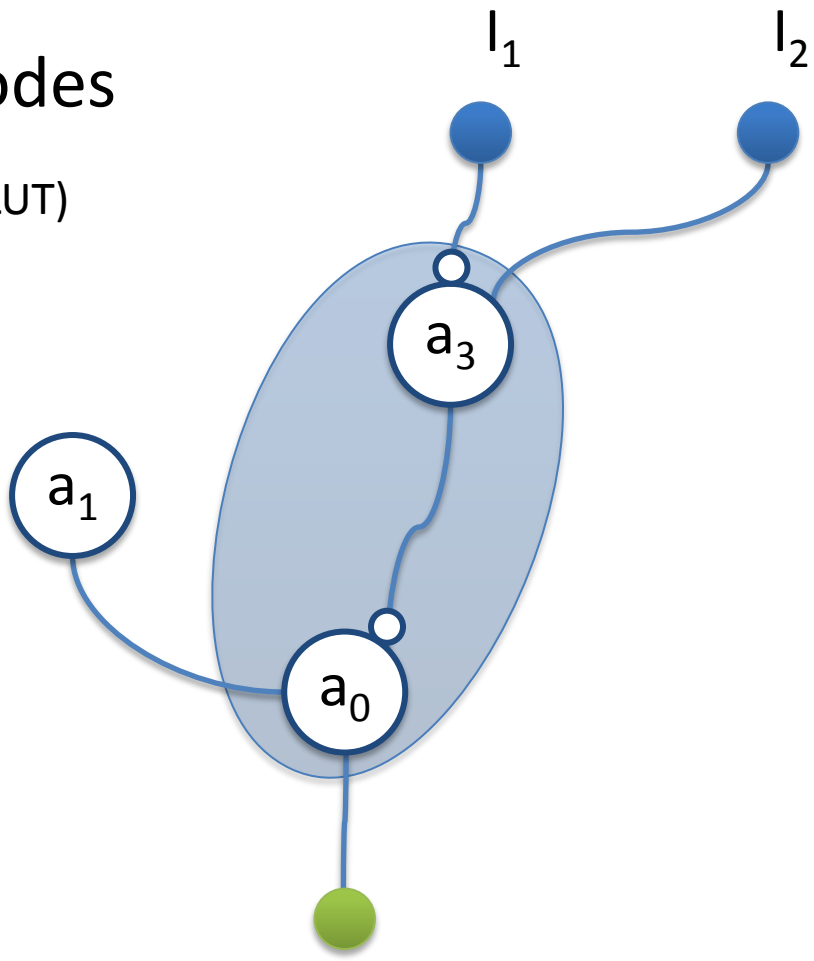
- Minimal depth mapping

1. Cone enumeration: Finding all feasible cones per node
2. Cone ranking: Selecting best feasible cone per node
3. Cone selection: Selecting cones that provide covering

Feasibility: LUT

Cone with 3 input nodes

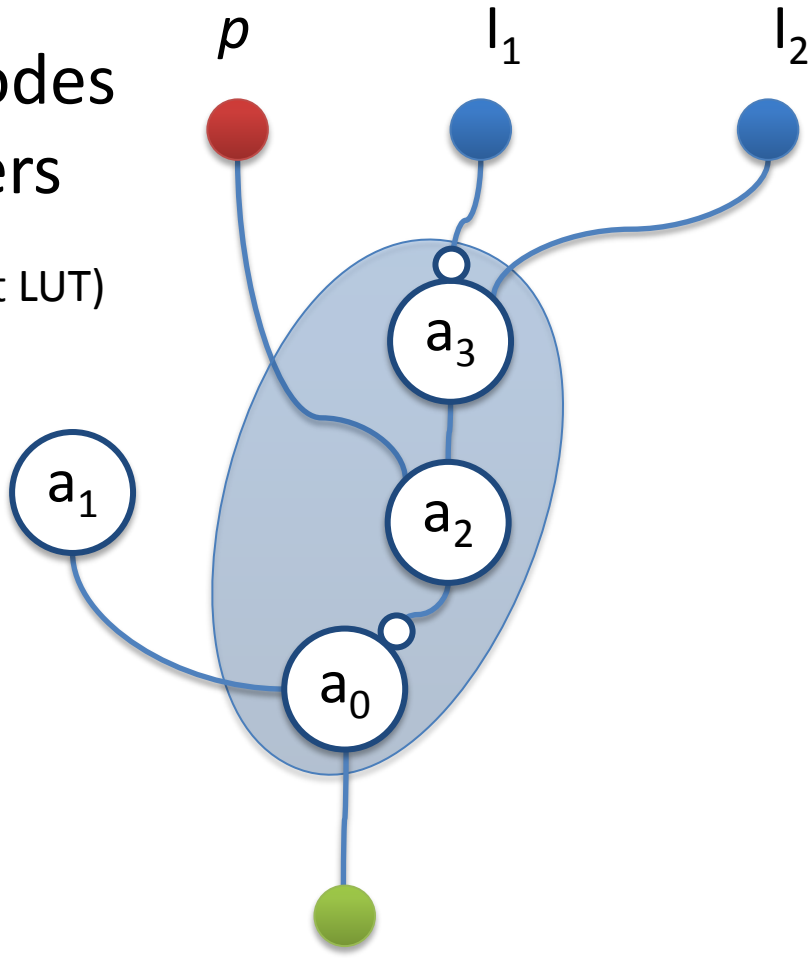
= LUT-feasible (3 input LUT)



Feasibility: TLUT

Cone with 3 input nodes that aren't parameters

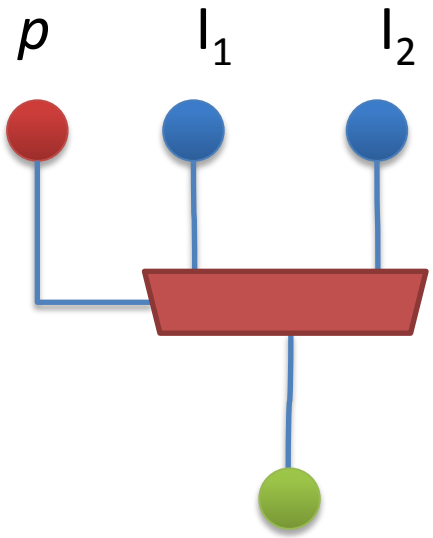
= TLUT-feasible (3 input LUT)

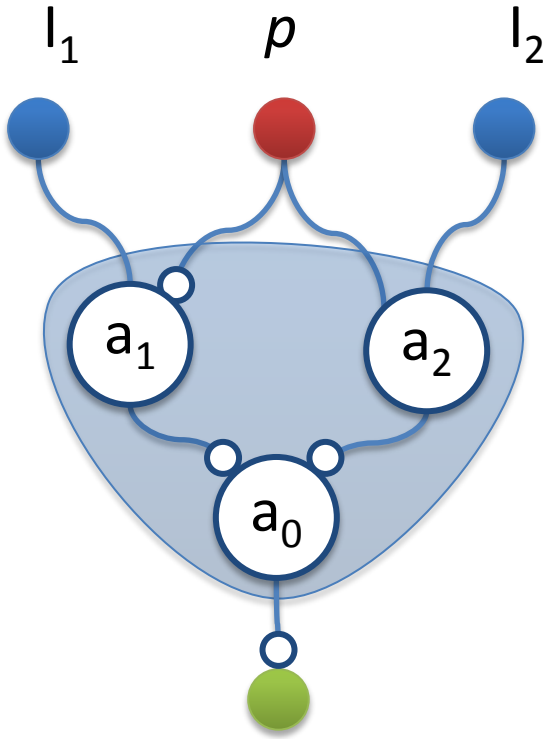


Feasibility: TCON

Equivalent to multiplexer controlled by function of parameters

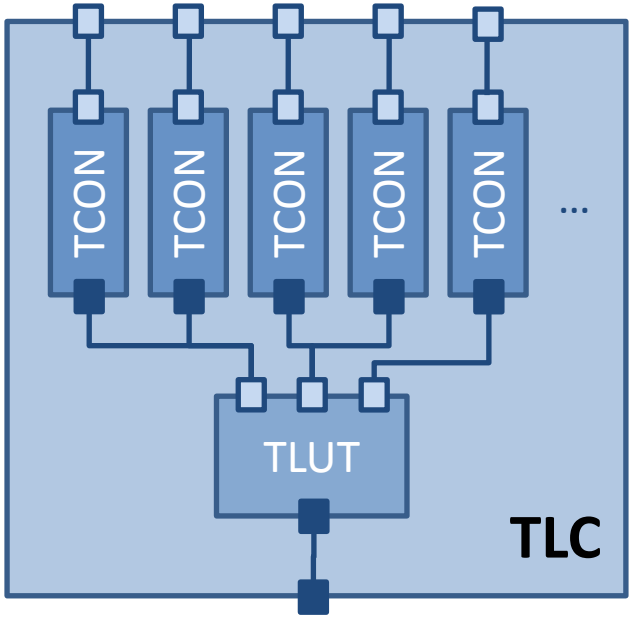
= TCON-feasible





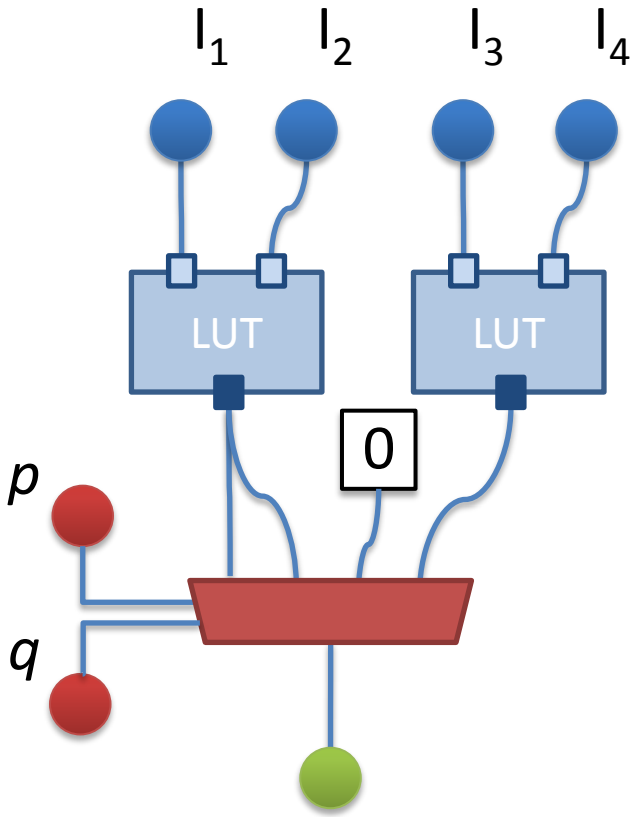
TLC supergate

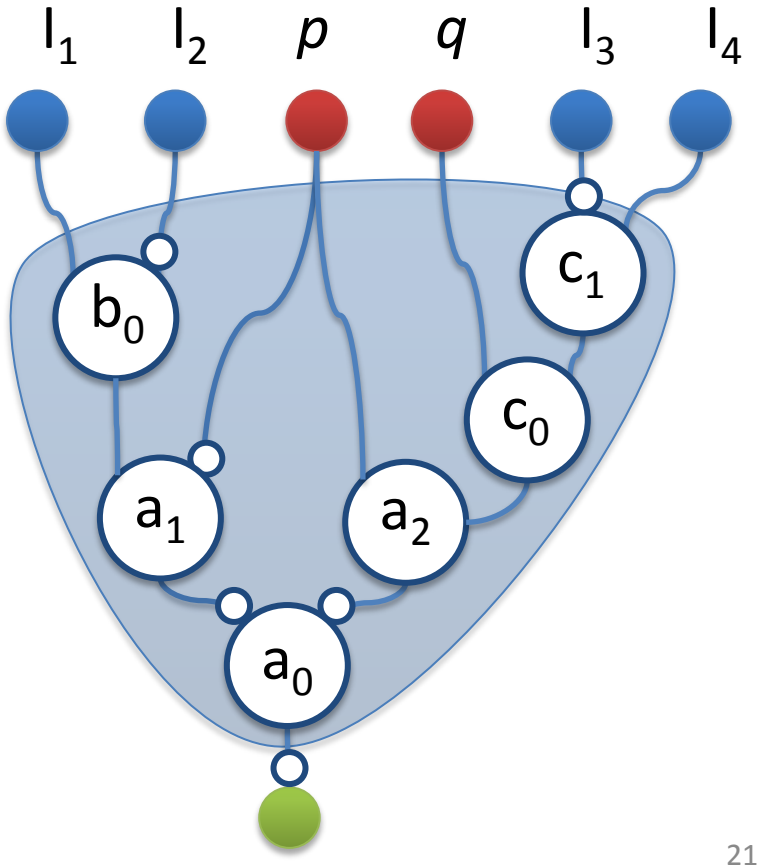
One TLUT with TCONs attached to its inputs



Feasibility: TLC supergate

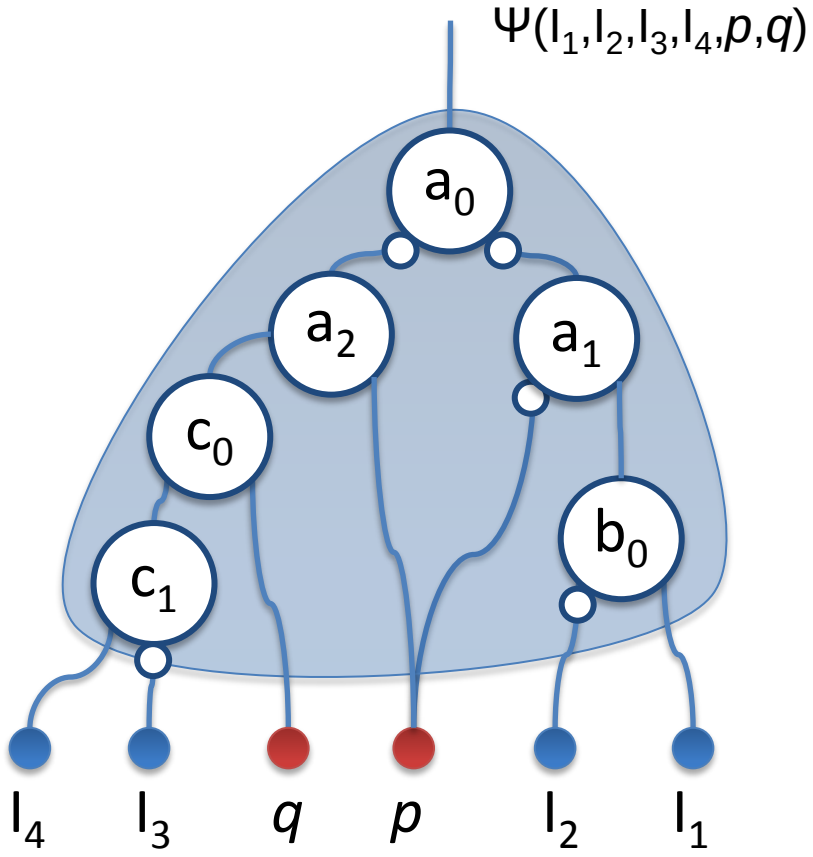
Equivalent to multiplexer controlled by function of parameters and LUTs at its inputs = TLC-feasible





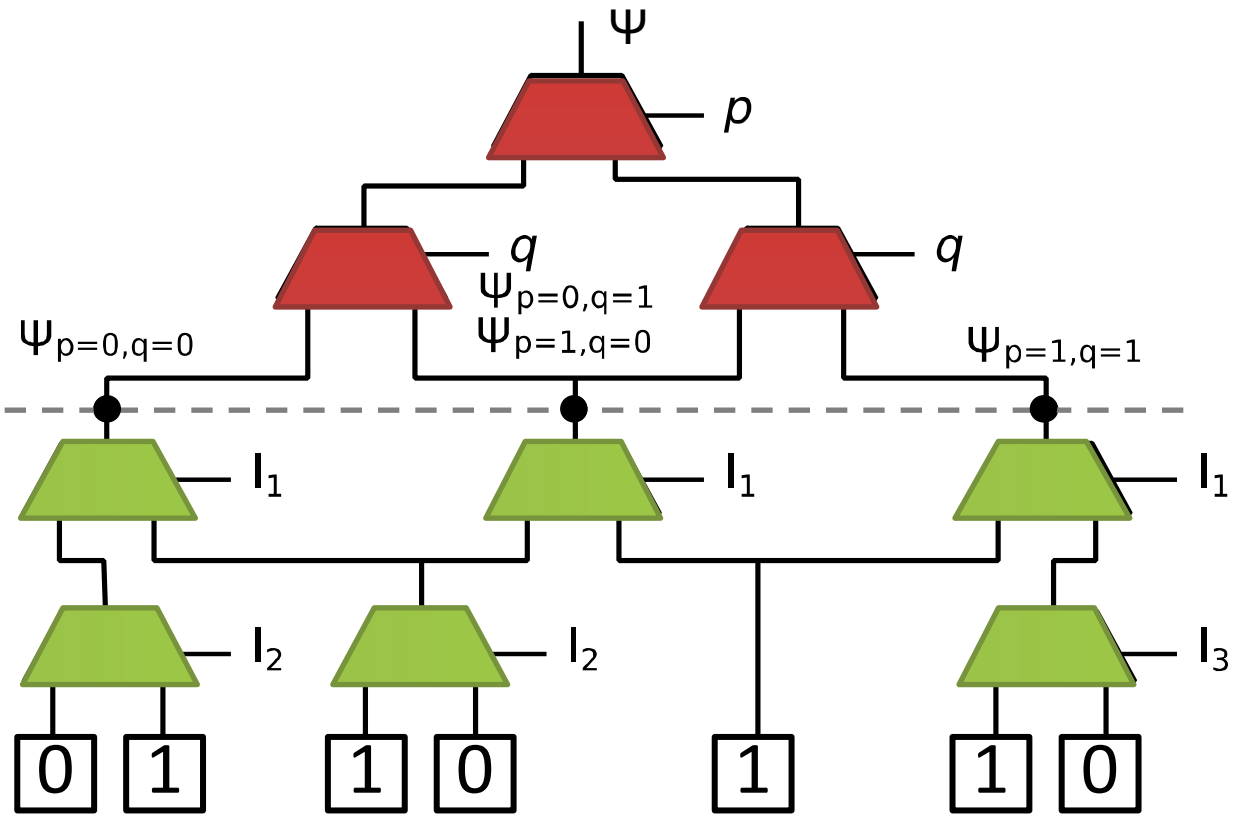
Feasibility calculation

Based on cone function: Ψ



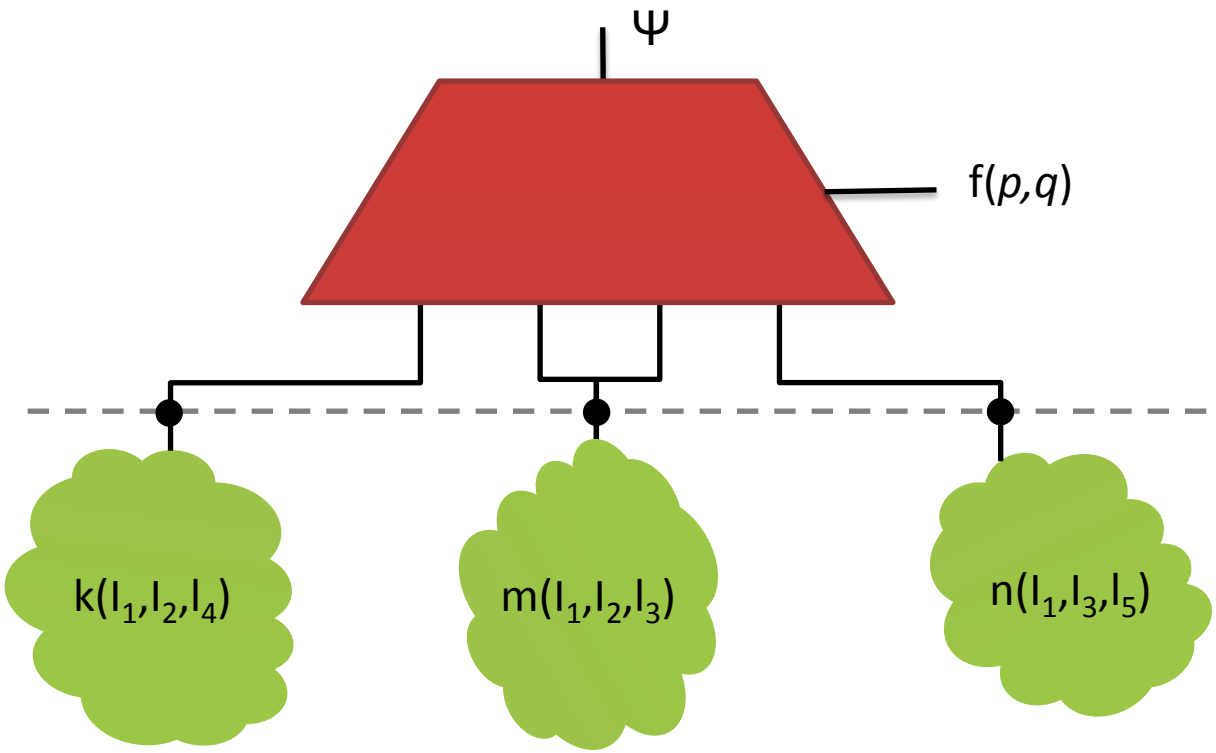
Feasibility calculation

Using Binary Decision Diagram of cone function



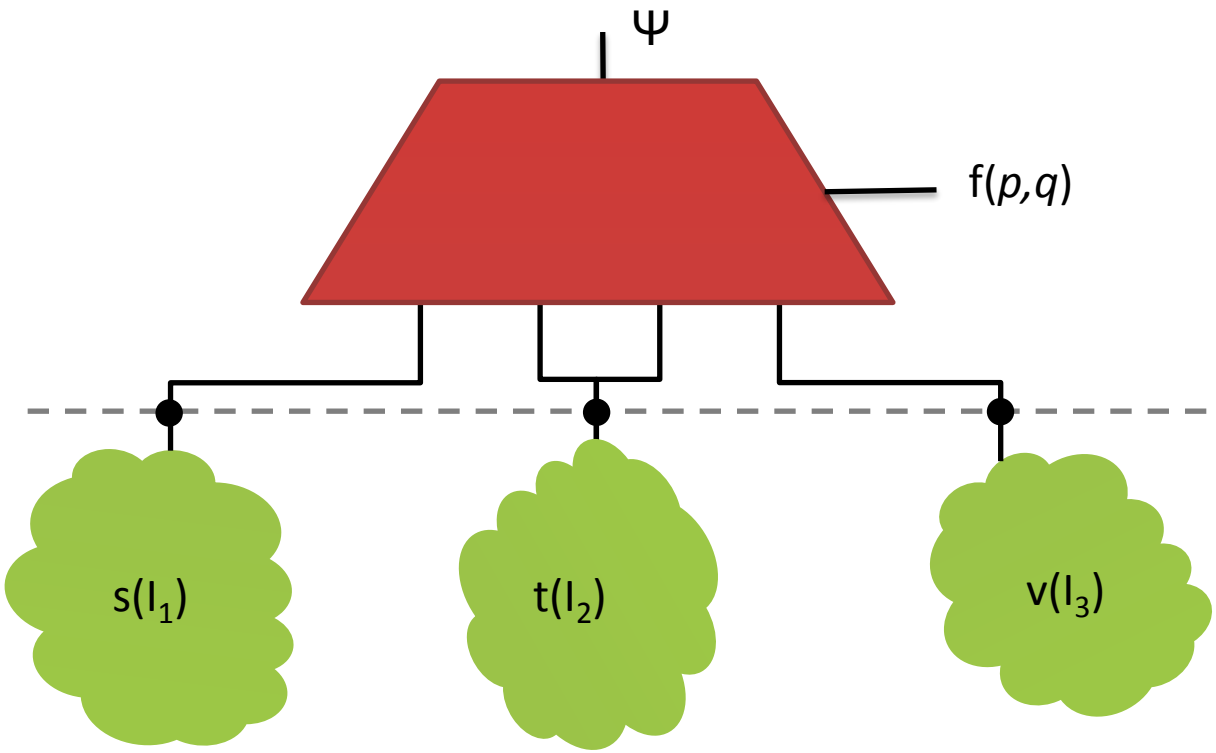
Feasibility calculation

Using Binary Decision Diagram of cone



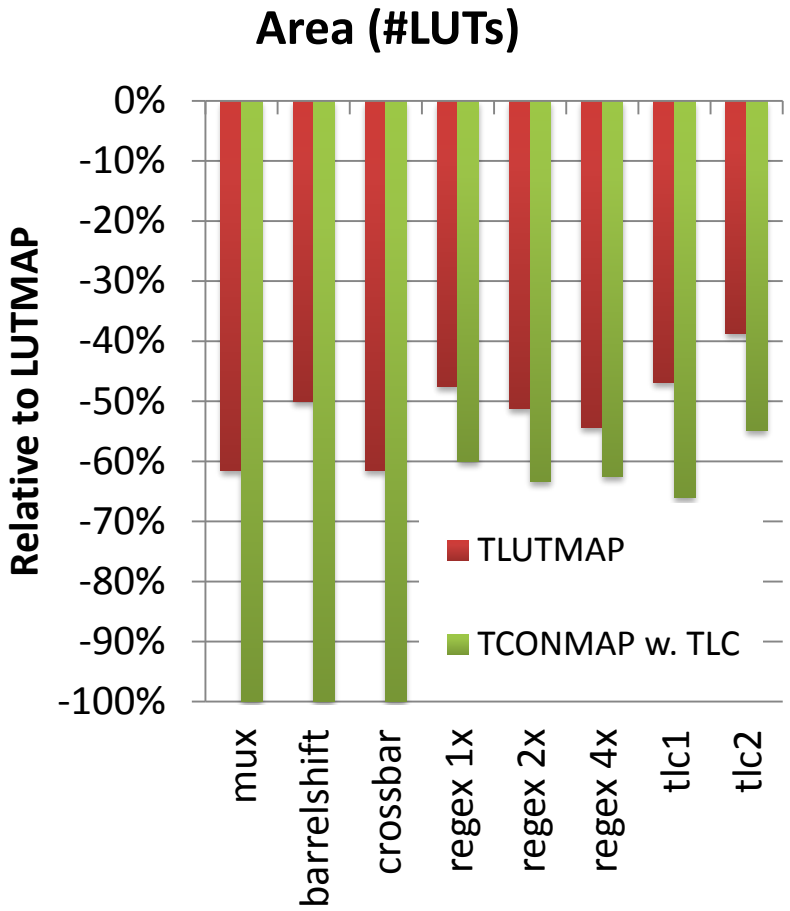
Feasibility calculation

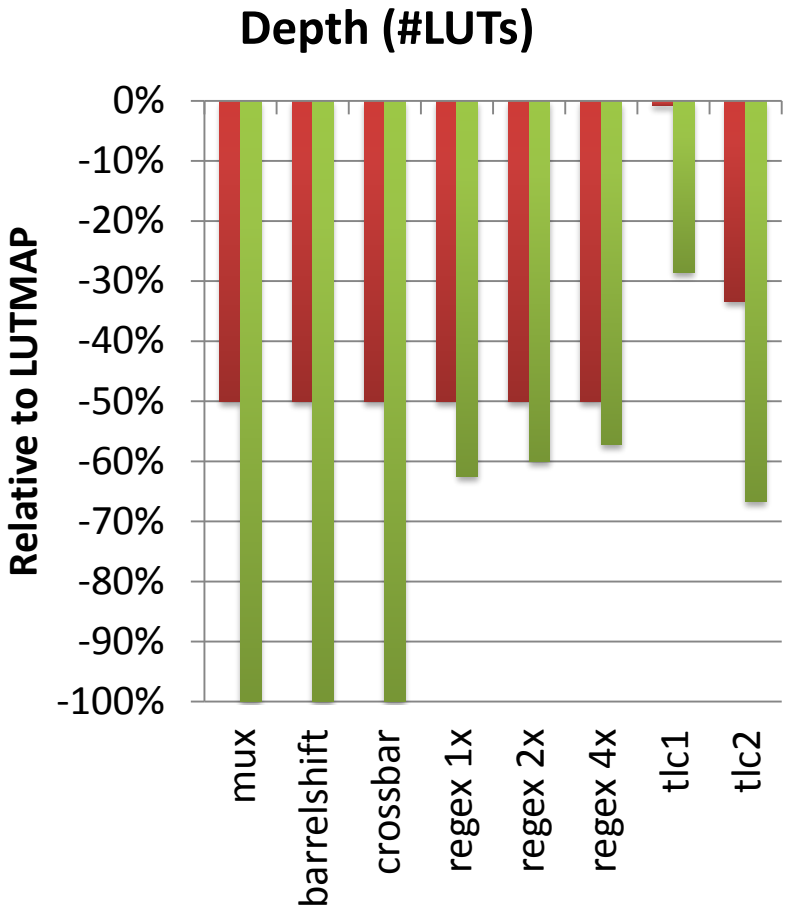
Using Binary Decision Diagram of cone



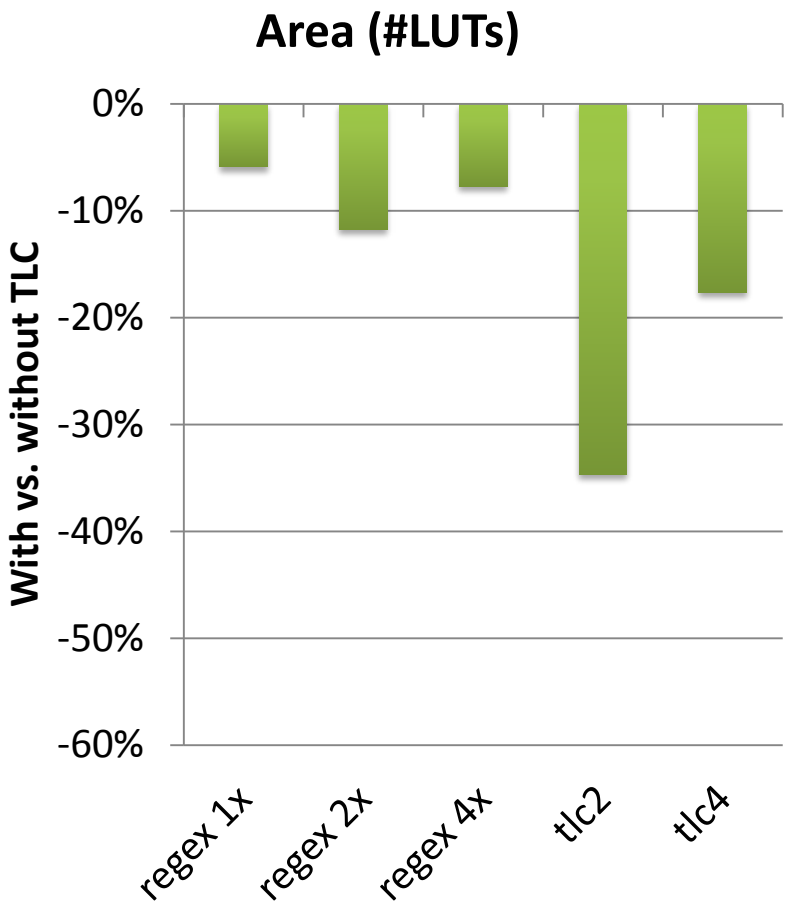
EXPERIMENTAL RESULTS

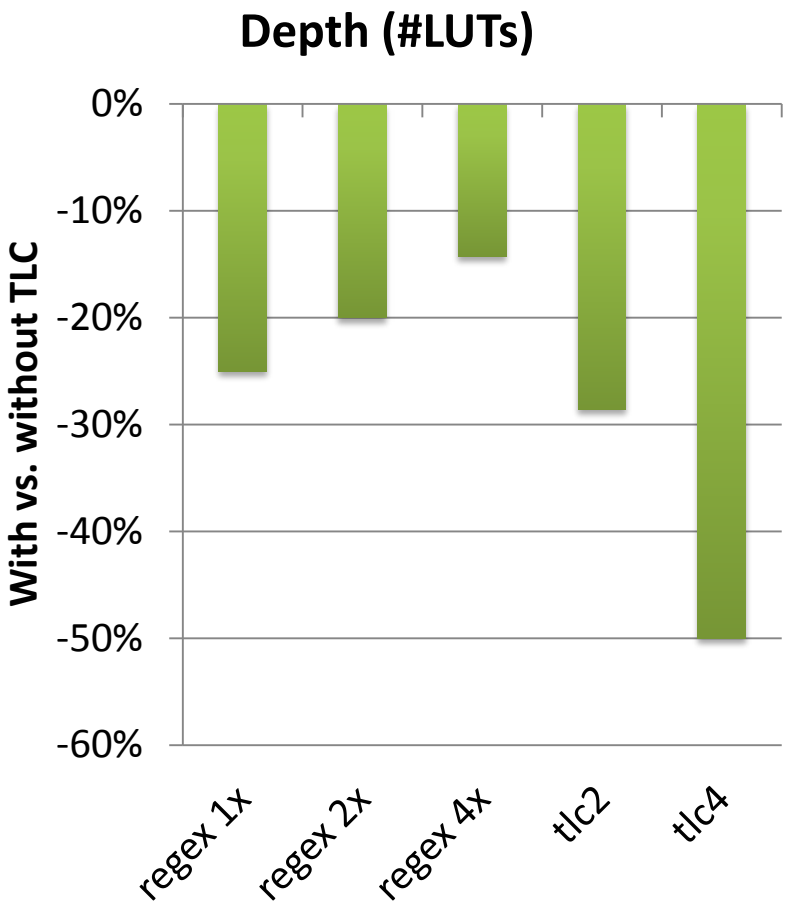
Area and depth



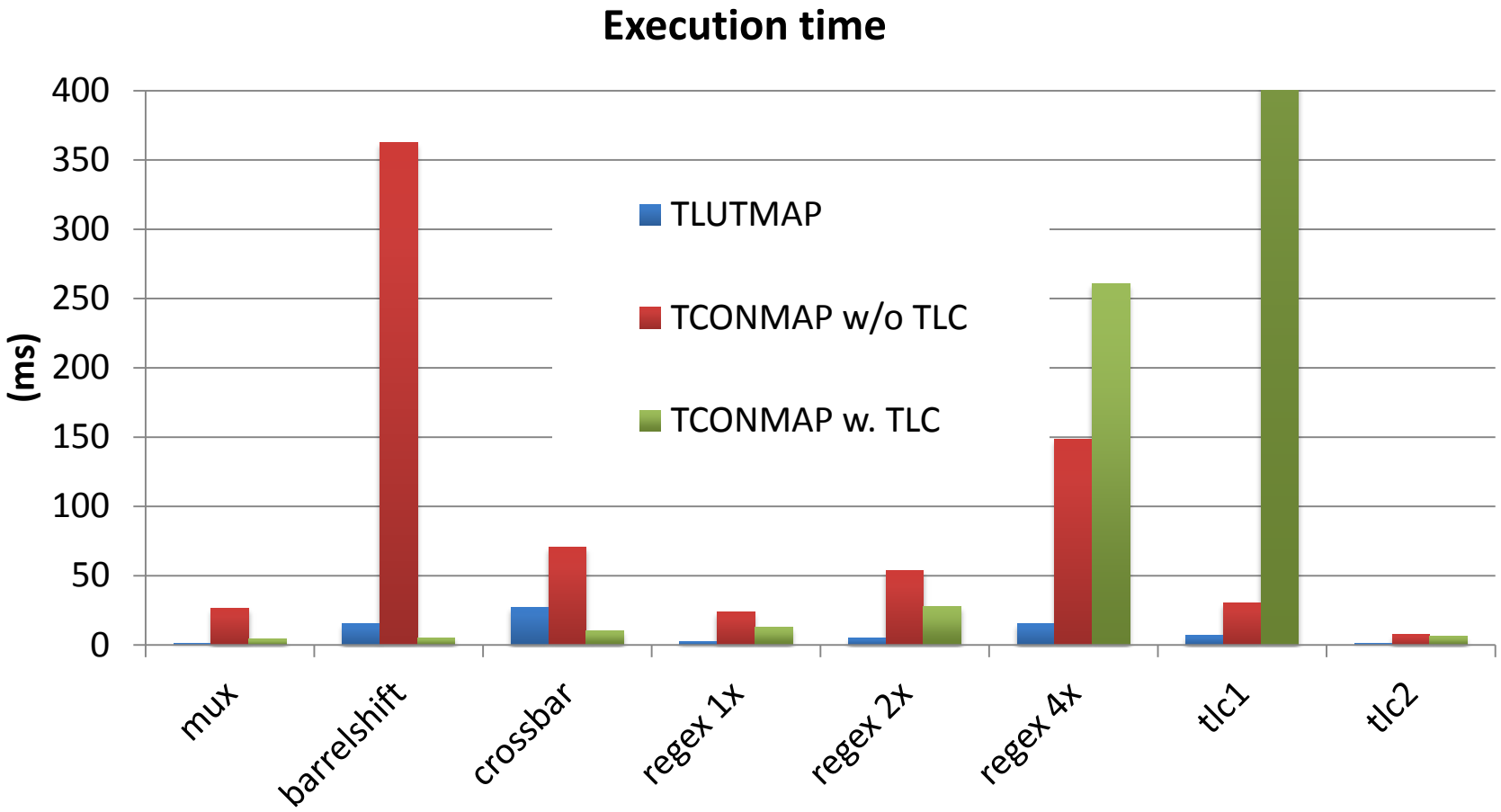


TLC supergate





Execution time and scaling behaviour



Conclusion

- Automatically map functionality to reconfigurable routing
- Creates **smaller** and **faster** mapping results

- Part of new toolflow to quickly create specialized configurations

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Acknowledgement

- Supported by European Commission FP7 project:

- The author is supported by a Ph.D. grant of the FWO-Vlaanderen