

UNITED KINGDOM · CHINA · MALAYSIA

### An Efficient Hardware Architecture of the Optimised SIFT Descriptor Generation

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### **Overview**

- Background Introduction
- Motivation of Work
- □ SIFT Algorithm
- Hardware Design
- Performance Evaluation
- Conclusions and Further Work



### **Background Introduction**

### Image Matching

### Applications

- Object or scene recognition
- Object localization and mapping
- Image fusion and registration
- 3D reconstruction







# **Motivation of Work**

### Challenges

- Descriptor Generation has become the bottleneck
- High throughput requirement for standalone real-time applications

### Objectives

- Improve descriptor generation efficiency
  --- by descriptor dimension reduction
- Computational complexity simplification
  - --- by LookUp Table Technique

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□ Stands for Scale Invariant Feature Transform

Extract highly distinctive invariant features

Scale and Rotation









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Illumination

3D viewpoint









Computation is highly complicated











#### Scale Space Construction



I(x, y)



·----→ σ↑















#### Extrema Detection



Maxima and Minima in a 3x3x3 neighbourhood

'X' represents the pixel to be compared with surrounding 26 pixels







#### Descriptor Generation of Original SIFT Algorithm





#### Descriptor Generation of our Optimised SIFT Algorithm



Polar Sampled Spatial Arrangement



Arrangement with Principal Orientation



8-bin Gradientorientation Histogram for Sub-region 3



2D Histogram for Sub-region 3

- Step 1: Arrangement of surrounding sub-regions
- Step 2: Arrangement of gradient histogram of each sub-region



#### Descriptor Generation of our Optimised SIFT Algorithm



 Step 3: Linking together the histograms of 9 subregions to generate a descriptor







### **Hardware Design**

### Overall Hardware Architecture

- Key Optimisation
  - LookUp Table

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#### > Overall Hardware Architecture



### Key Optimisation

#### LookUp Table







#### Gaussian Weighting Factor Controller



 $(x_c, y_c)$ : coordinates of centre pixel

 $(x_i, y_i)$ : coordinates of a pixel to be weighted





#### Centre Coordinate Calculation

Table 1. Offsets from the centre coordinates of sub-regions to thefeature point in both x and y directions

Sub- region	$\Delta x_{OR_i}$	$\Delta y_{OR_i}$		
1	$r * \cos(\theta_{po})$	$r * cos(\theta_{po})$ $r * sin(\theta_{po})$		
2	$\frac{\sqrt{2}}{2}r * (\cos(\theta_{po}) - \sin(\theta_{po})) \qquad \frac{\sqrt{2}}{2}r * (\cos(\theta_{po}) + \sin(\theta_{po}))$			
3	$-\mathbf{r} * sin(\theta_{po})$	$r * \cos(\theta_{po})$		
4	$-\frac{\sqrt{2}}{2}r*(\cos(\theta_{po})+\sin(\theta_{po}))$	$\frac{\sqrt{2}}{2}r*(\cos(\theta_{po})-\sin(\theta_{po}))$		
5	$-r * \cos(\theta_{po})$	$-\mathbf{r} * sin(\theta_{po})$		
6	$\frac{\sqrt{2}}{2}r * (\sin(\theta_{po}) - \cos(\theta_{po}))$	$-\frac{\sqrt{2}}{2}r*(\cos(\theta_{po})+\sin(\theta_{po}))$		
7	$r * sin(\theta_{po})$	$-r * \cos(\theta_{po})$		
8	$\frac{\sqrt{2}}{2}r * (\cos(\theta_{po}) + \sin(\theta_{po}))$	$\frac{\sqrt{2}}{2}r * (\sin(\theta_{po}) - \cos(\theta_{po}))$		
9	$0 \\ (x_{\theta_{p_0}}, y_{\theta_{p_0}}) : cc$	0 ordinates of the feature point		
	Po Po			





 $(x_{OR_i}, y_{OR_i})$ : centre coordinates of surrounding sub-regions



Centre Coordinate Calculation



### **Performance Evaluation**

### Matching Performance

Matching results



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#### Matching performance comparison





#### Hardware Efficiency

### Table 1. Hardware Resource Usage and ThroughputComparison of Different Hardware Designs

	Y. Lin's [2010]	K. Mizuno's [2010]			
		High-accuracy Mode	High-speed Mode	[2012]	Our design
Frame Size	N/A	VGA			
Frequency (MHz)	200	50		100	100
Registers		23,2	23,247 <b>29,453</b>		29,453
LUTs	N/A	32,592		N/A	64,701
DSP		258			107
Memory Usage (Mb)		0.87	0.67	4.86	3.84
Time Consumption per Descriptor (us)	15.315	N/A		33.1	7.57
Frame Rate (fps)	N/A	32	56	30	at least 60



# **Conclusions and Further Work**

### Conclusions

- 7.57 us per descriptor @100MHz
- 132,100 descriptors per second
- 2,200 descriptors/frame @60 VGA fps
- Real-time processing of even higher resolution images

#### Further Work

- FPGA prototype of a dual-camera image matching system
- A real-time vision system for visual prosthesis simulator

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**Overview** 



# Thank you!

