



Microelectronics System Design Group

Intra-chip Physical Parameter Sensor for FPGAs using Flip-Flop Metastability

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30th August 2012

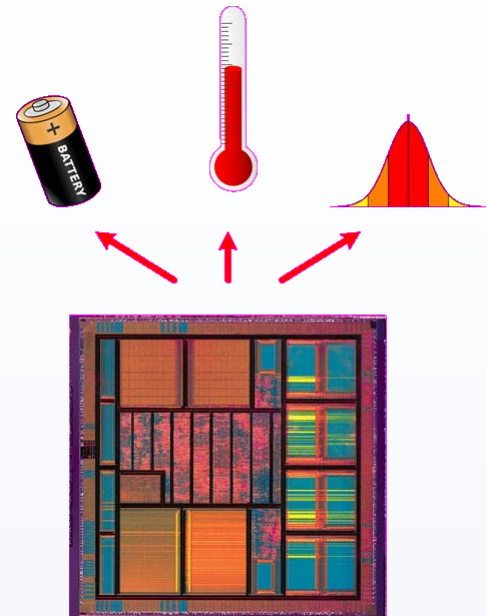
Presentation Overview

- Introduction
- Ring Oscillator Sensing
- Proposed Sensor
- FPGA Measurements
- Conclusion

Introduction

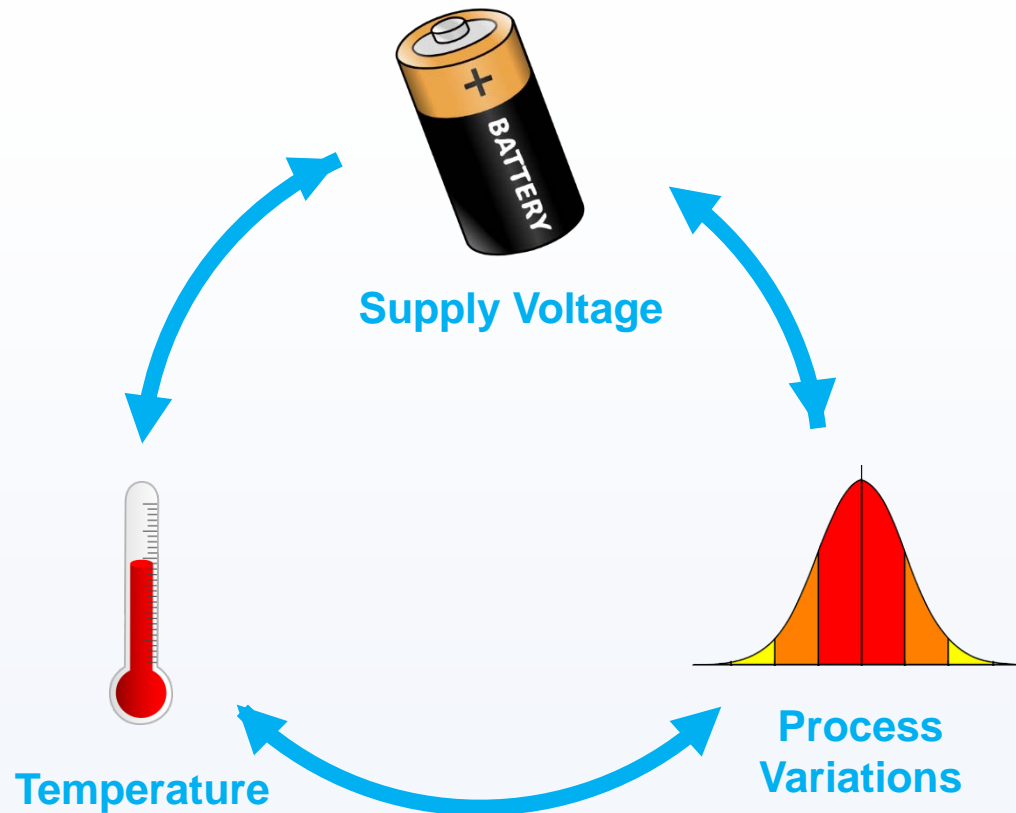
- **Physical parameter sensing in FPGAs:**

1. Dynamic power and thermal management
2. Development of power and thermal models
3. Variation-aware component placement
4. Monitoring and performance profiling



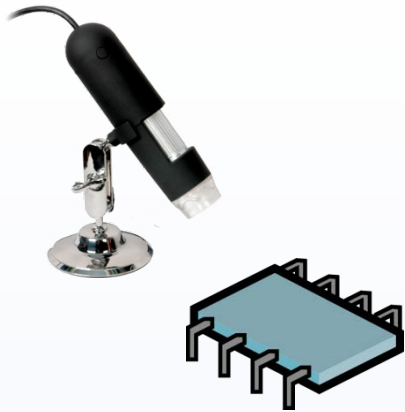
Introduction

- Intra-chip physical parameters are strongly interlinked.



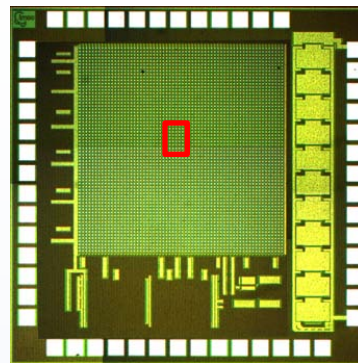
Introduction

- Physical parameter sensing in FPGAs:



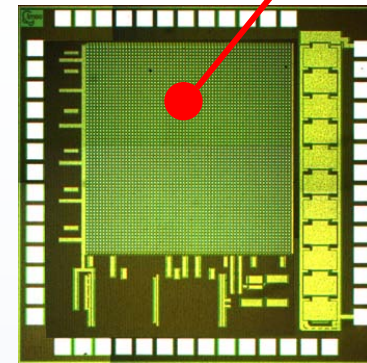
External

1



Built-in Sensors

2



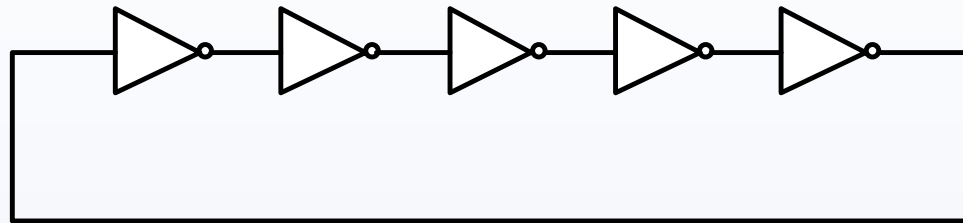
Soft Sensors

3

Introduction

- **Ring Oscillators:**

- Oscillation frequency inversely proportional to element delay
- Higher VDD \rightarrow lower element delay \rightarrow higher frequency



$$f = \frac{1}{2 \times n \times t_d}$$

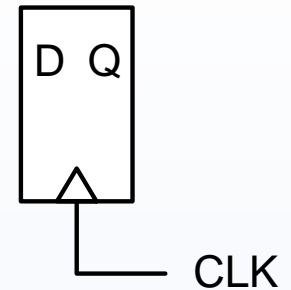
n : number of elements in loop

t_d : delay of single element

Proposed Sensor

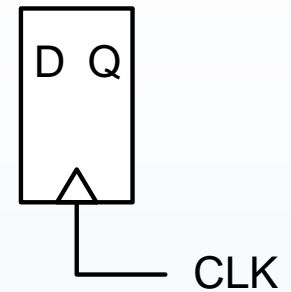
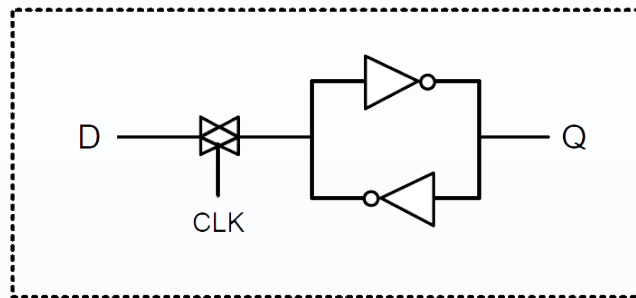
- **Flip-flop Metastability:**

- When the setup and hold time conditions of a flip-flop are not met, the flip-flop may become **metastable**.
- A metastable flip-flop will take extra time to decide whether to go logic high or low.
- Extra decision time = higher clock-to-q delay



Proposed Sensor

- **Flip-flop Metastability:**



$$Q(t) = Q' \times e^{t/\tau}$$

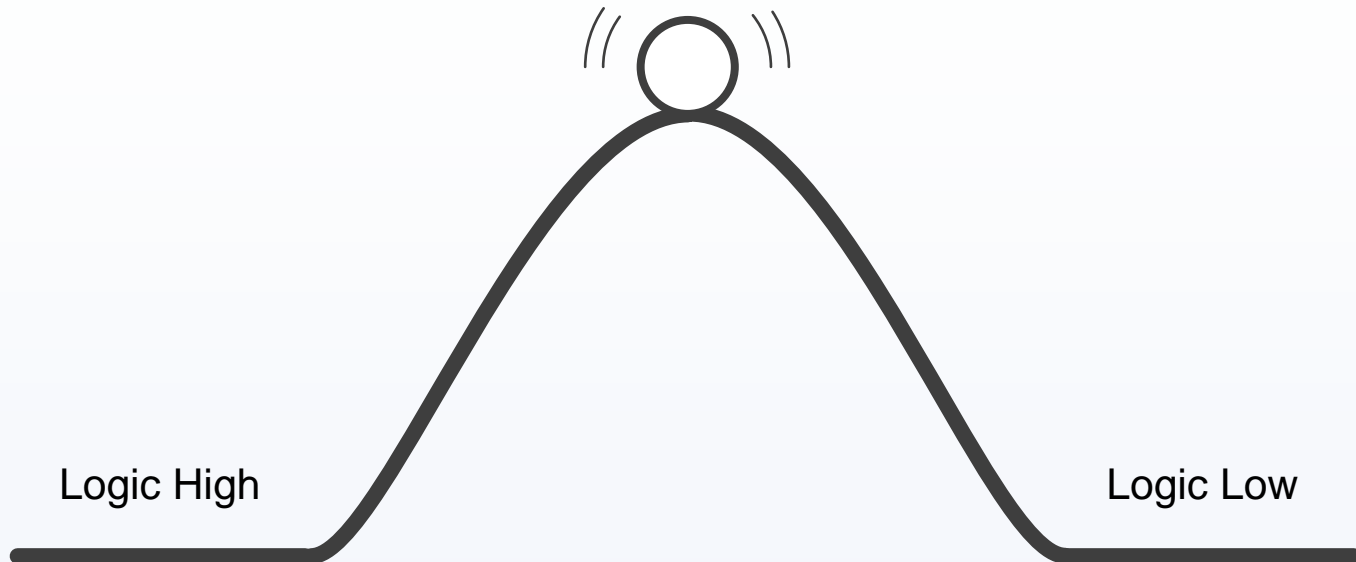
- The time constant τ is a function of the flip-flop's transconductance.

Proposed Sensor

- **Flip-flop Metastability:**
 - The probability that the flip-flop's clock-to-q delay will exceed t seconds depends exponentially on the value of the time constant τ .

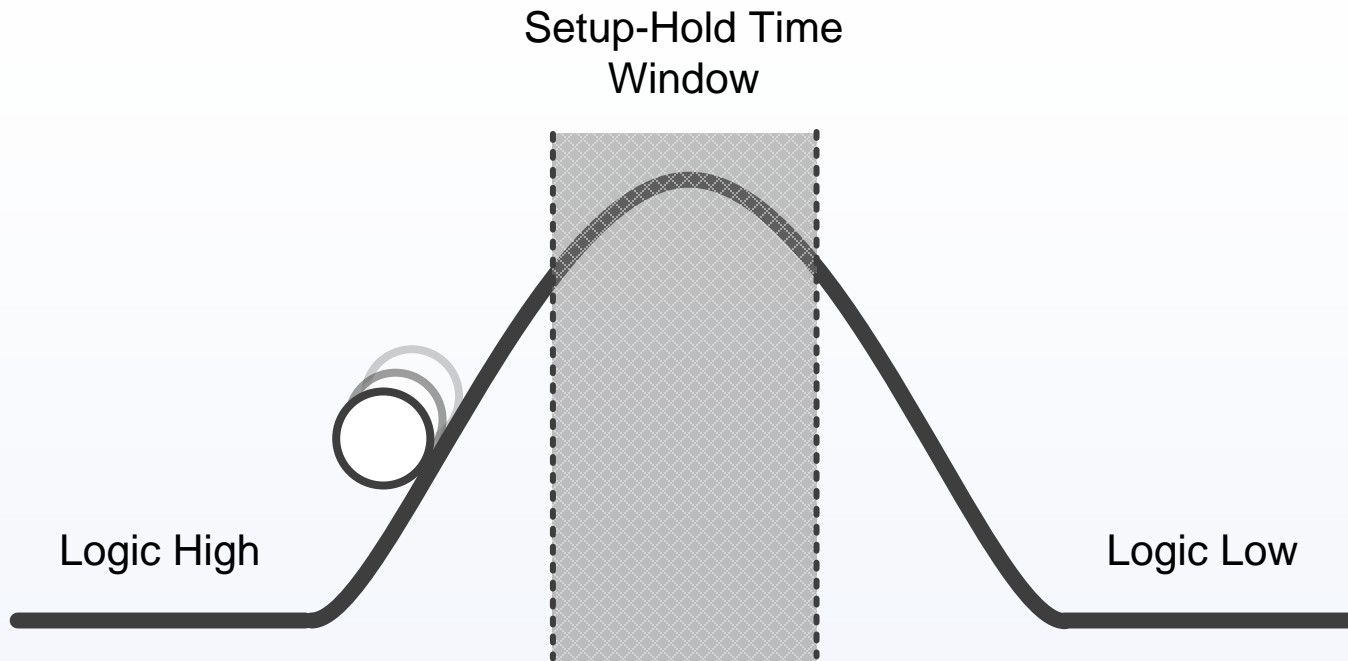
Proposed Sensor

- **Flip-flop Metastability:**



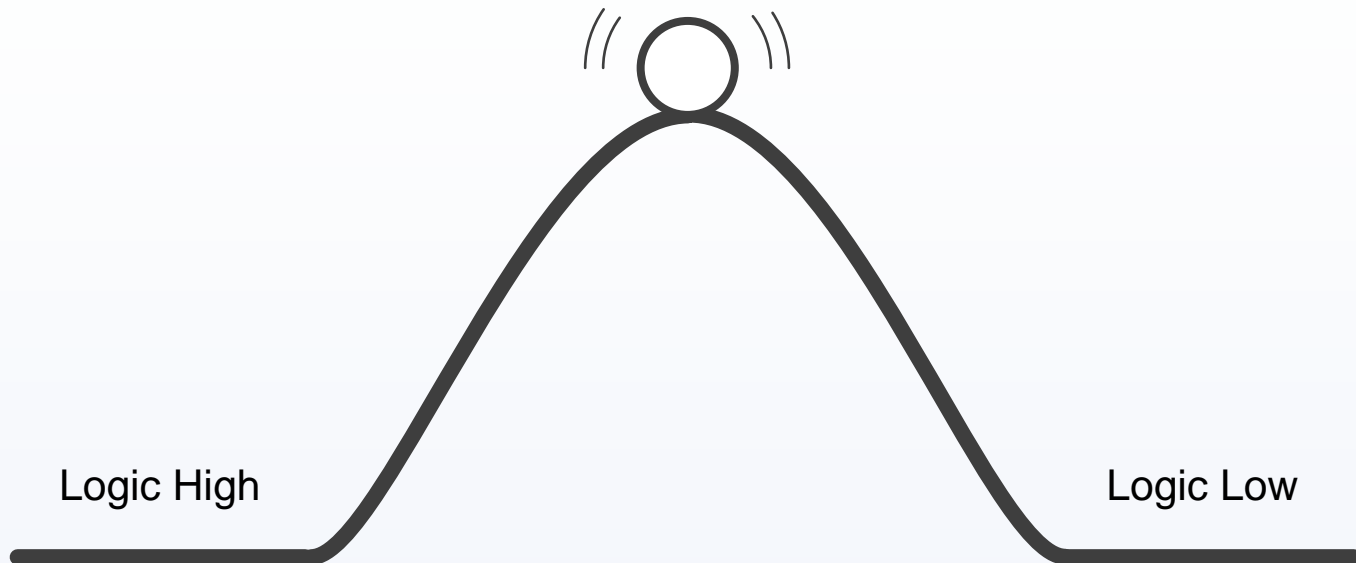
Proposed Sensor

- **Flip-flop Metastability:**



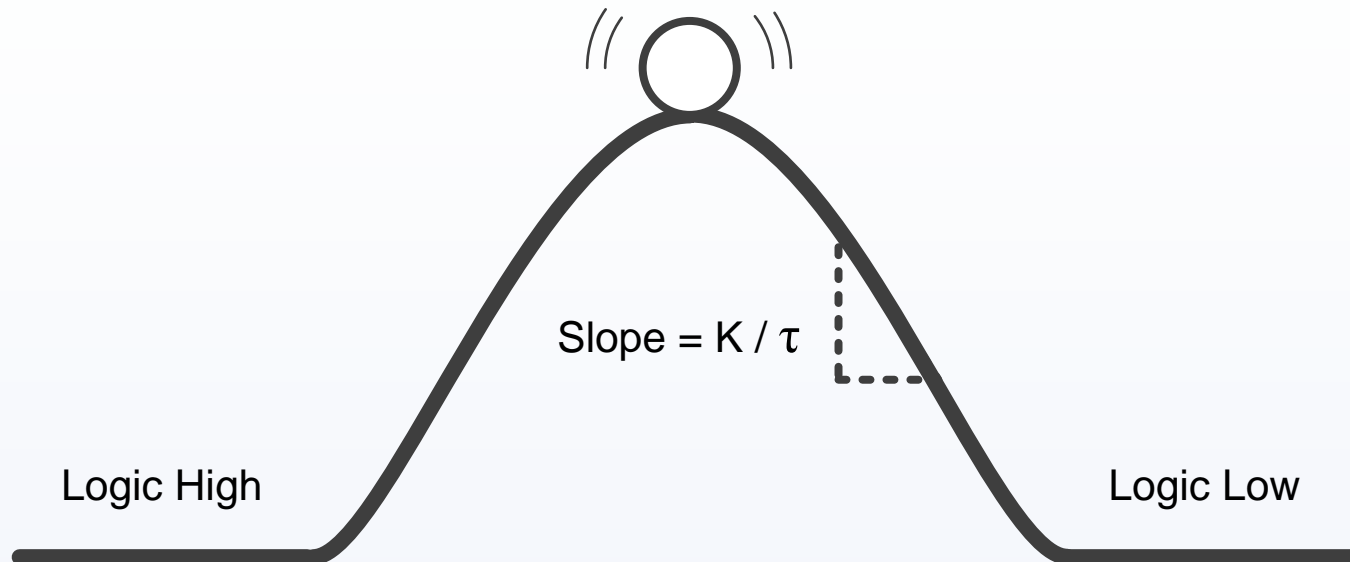
Proposed Sensor

- **Flip-flop Metastability:**



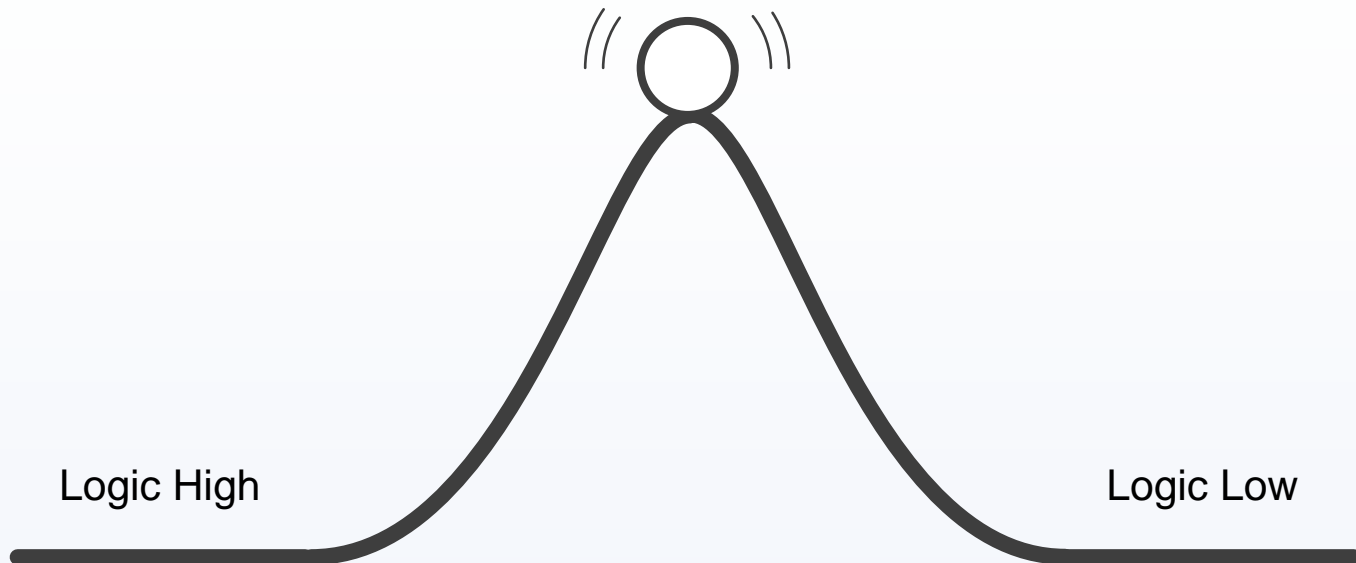
Proposed Sensor

- **Flip-flop Metastability:**



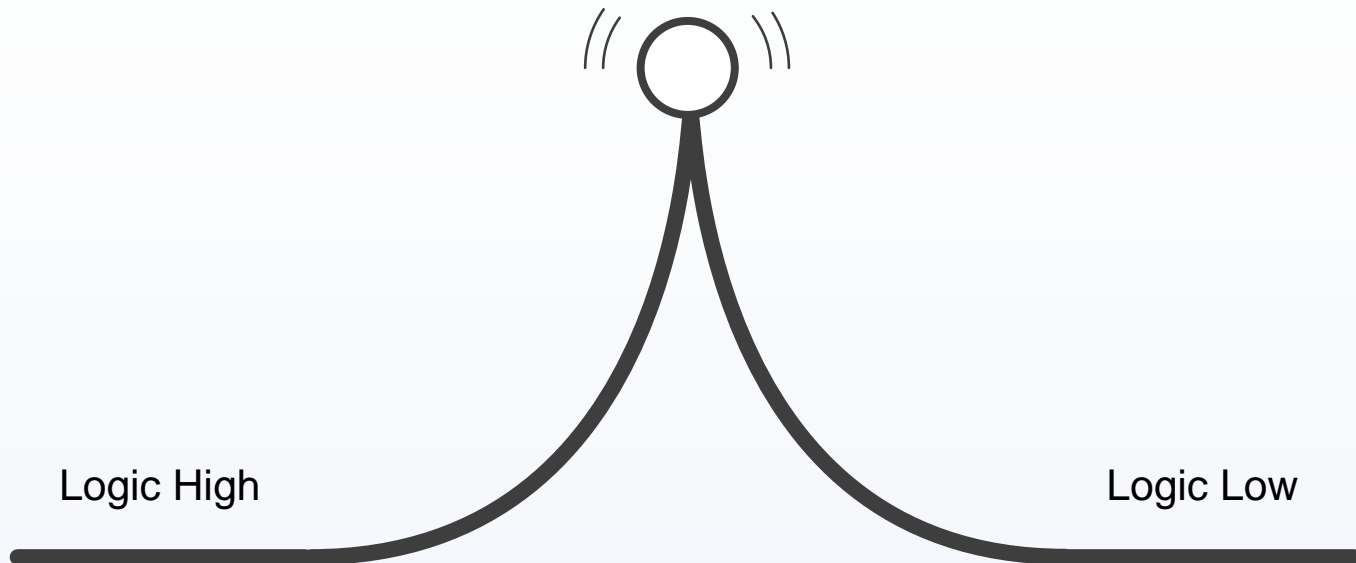
Proposed Sensor

- **Flip-flop Metastability:**



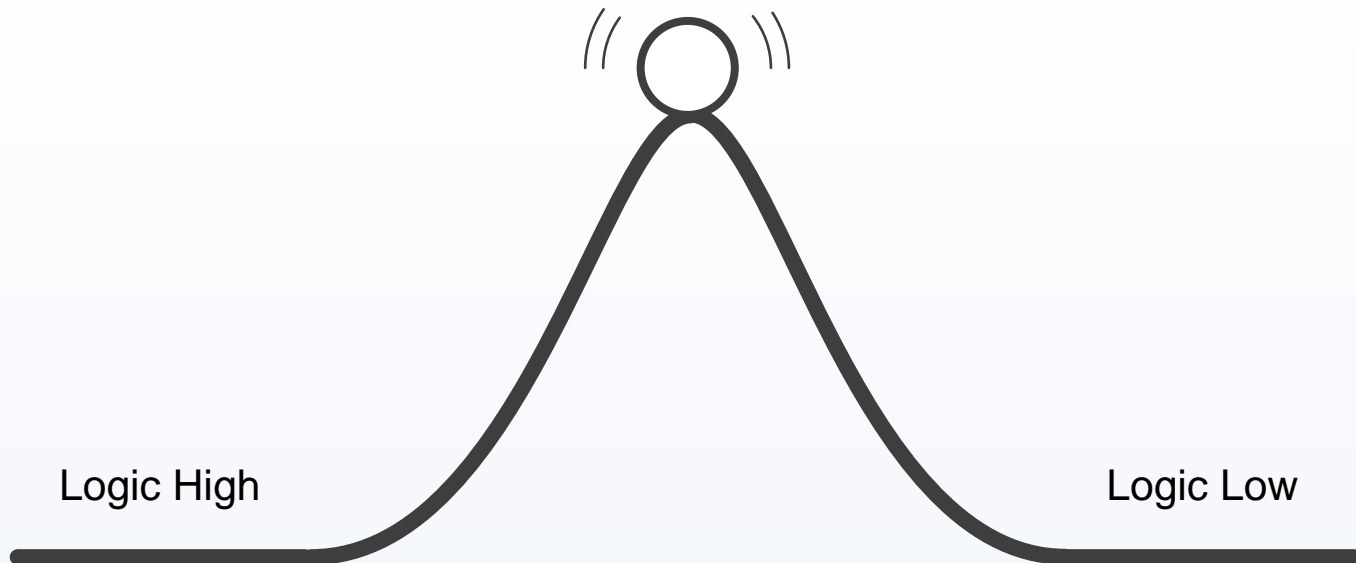
Proposed Sensor

- **Flip-flop Metastability:**



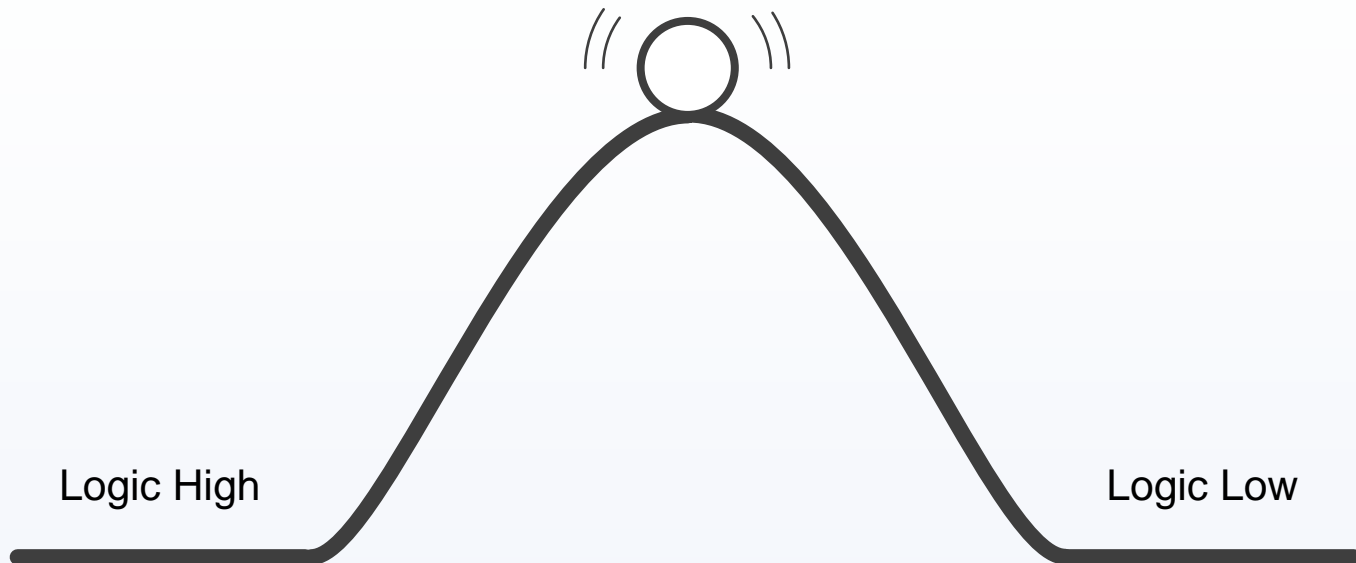
Proposed Sensor

- **Flip-flop Metastability:**



Proposed Sensor

- **Flip-flop Metastability:**

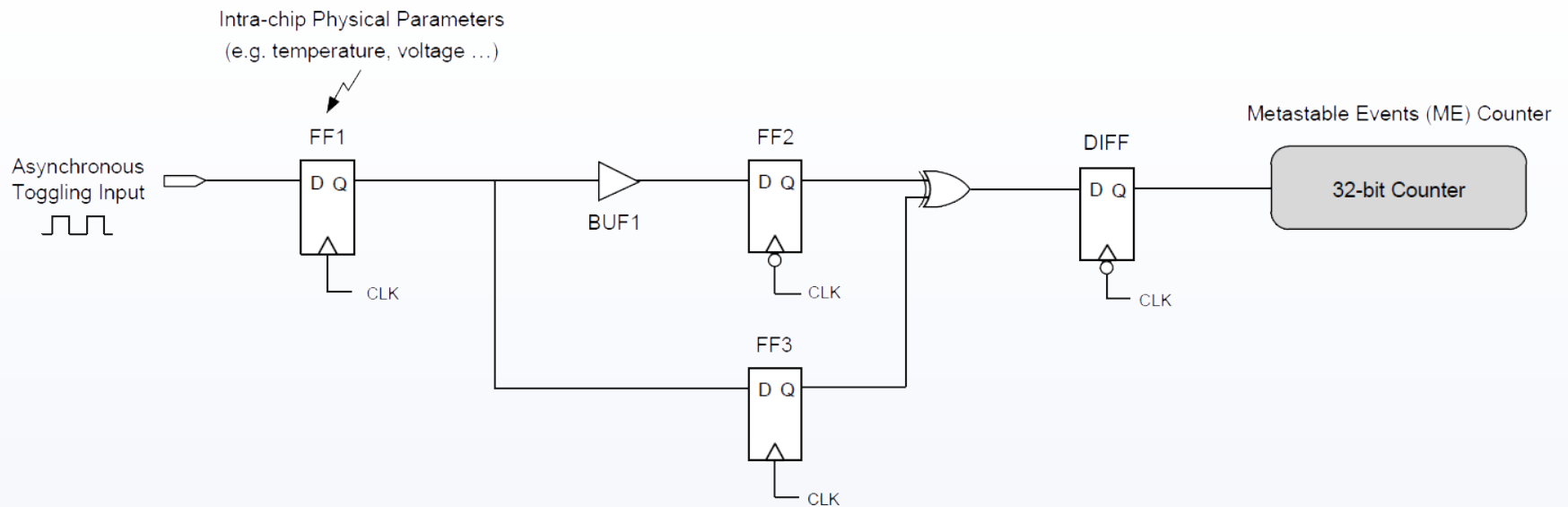


Proposed Sensor

- **Flip-flop Metastability:**
 - Tau (the slope of the hill) is a function of the cross-coupled gates transconductance.
 - Tau is influenced by physical parameter variations similar to propagation delay.

Proposed Sensor

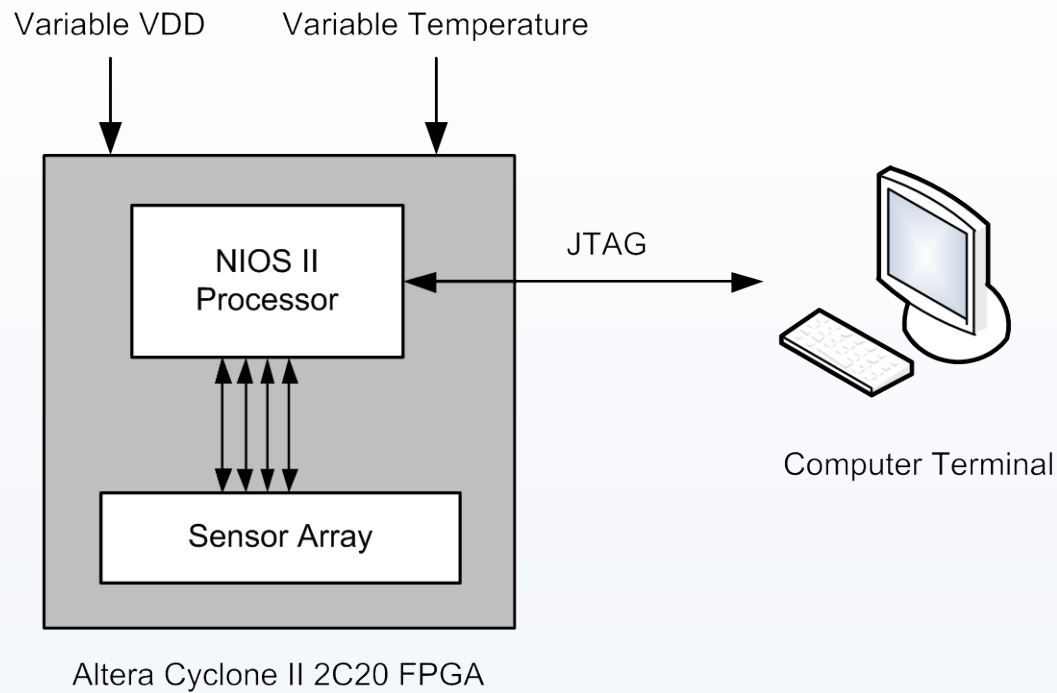
- Proposed Design:



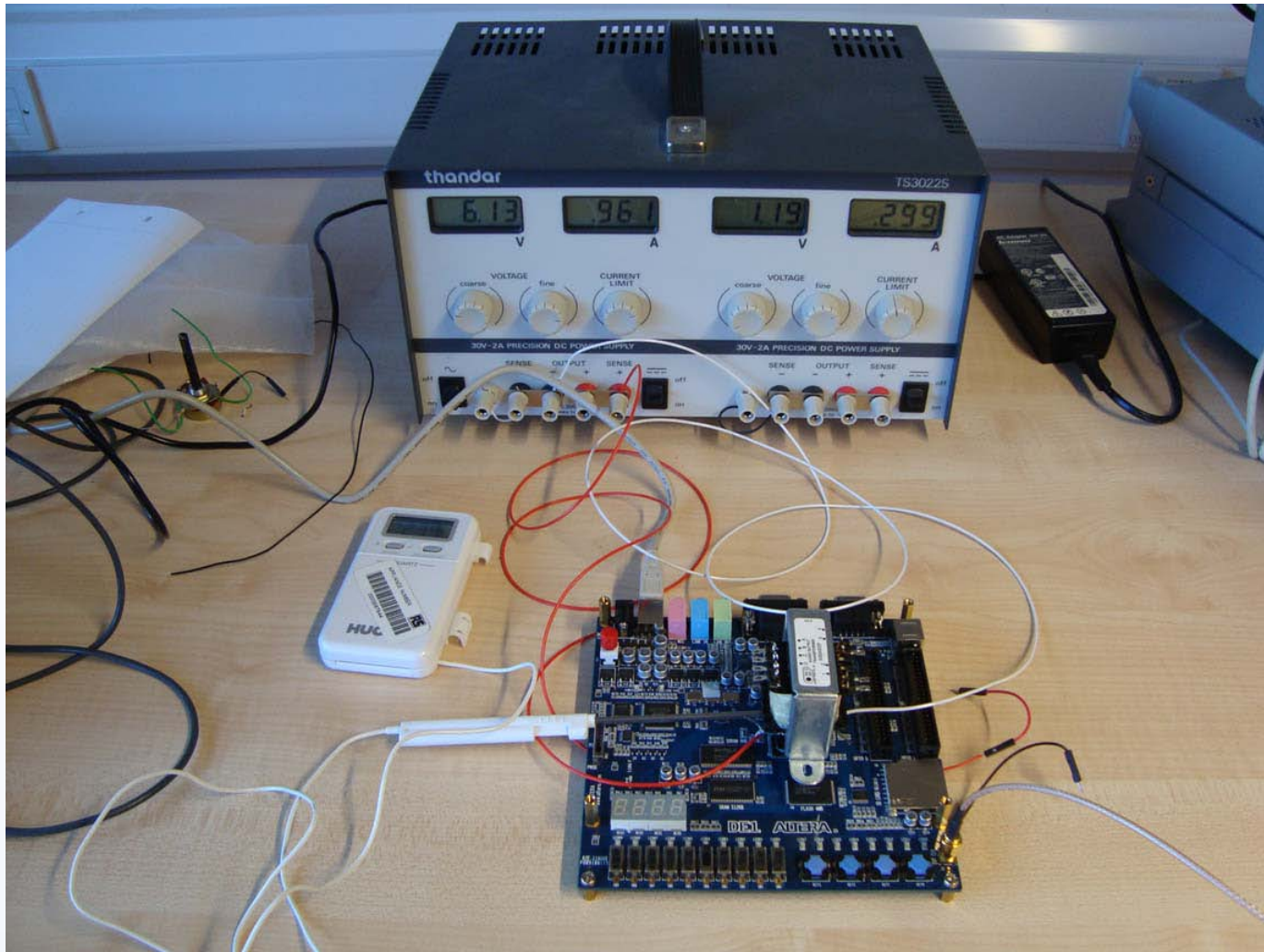
$$\text{Count} = n \times K \times e^{Sp}$$

FPGA Measurements

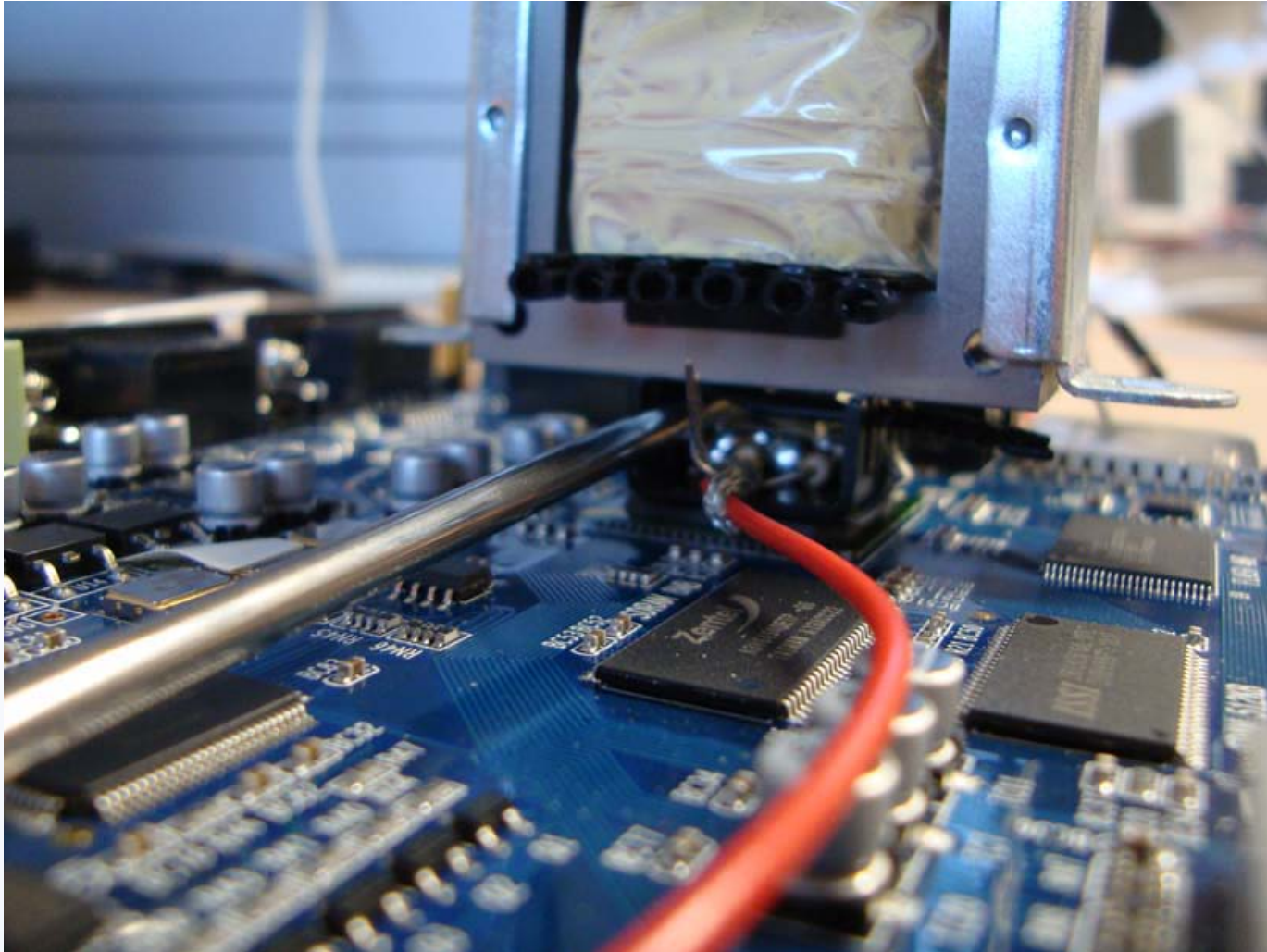
- **Sensor characterization system:**



FPGA Measurements



FPGA Measurements



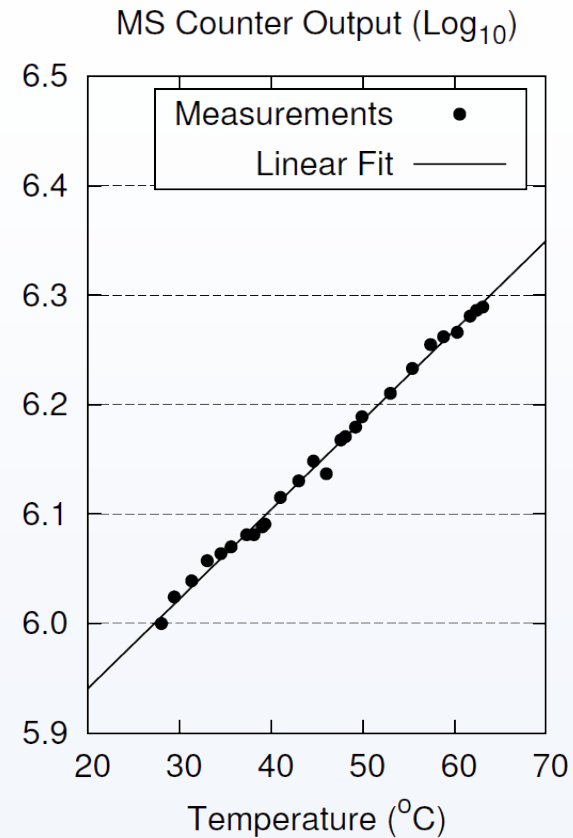
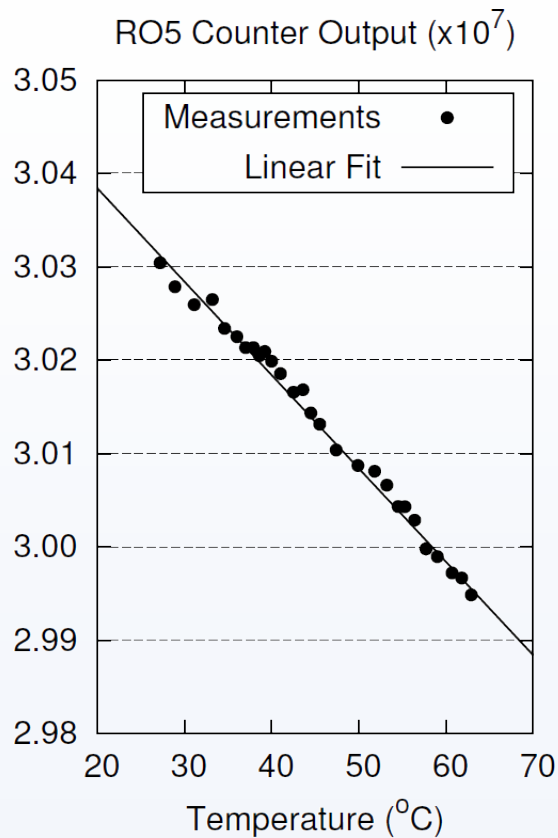
FPGA Measurements

- **Compared Sensors:**

Sensor	Description	LUTs	FFs
R05	5-stage RO with 3 decimation stages	9	5
R011	11-stage RO with 3 decimation stages	15	5
R017	17-stage RO with 3 decimation stages	21	5
MS	metastability-based sensor (proposed)	2	4

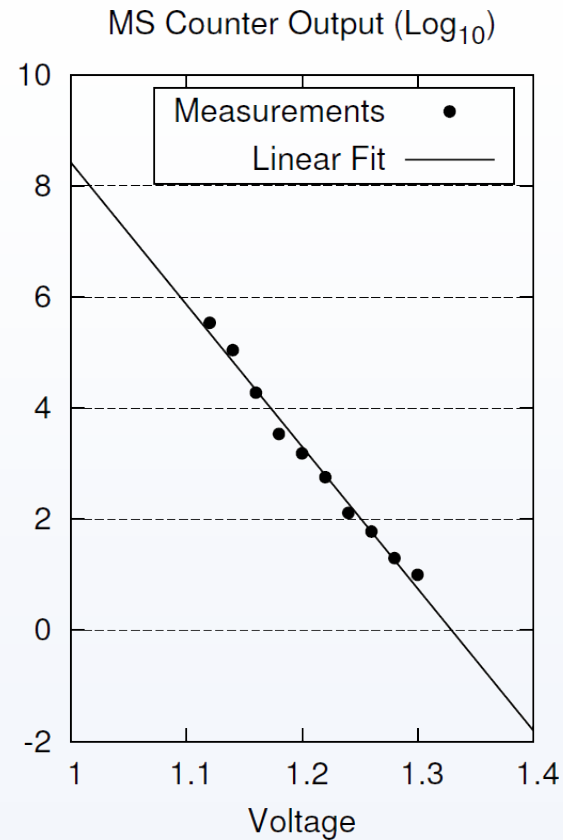
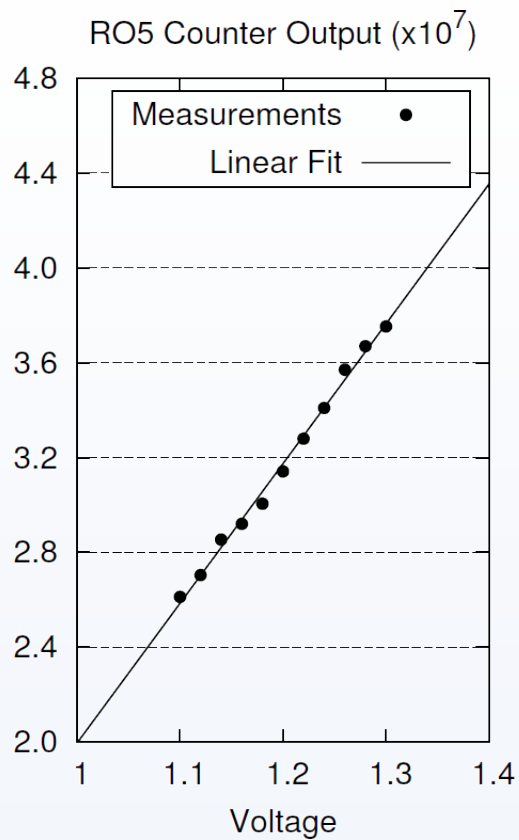
FPGA Measurements

- **Output Response (Temperature):**



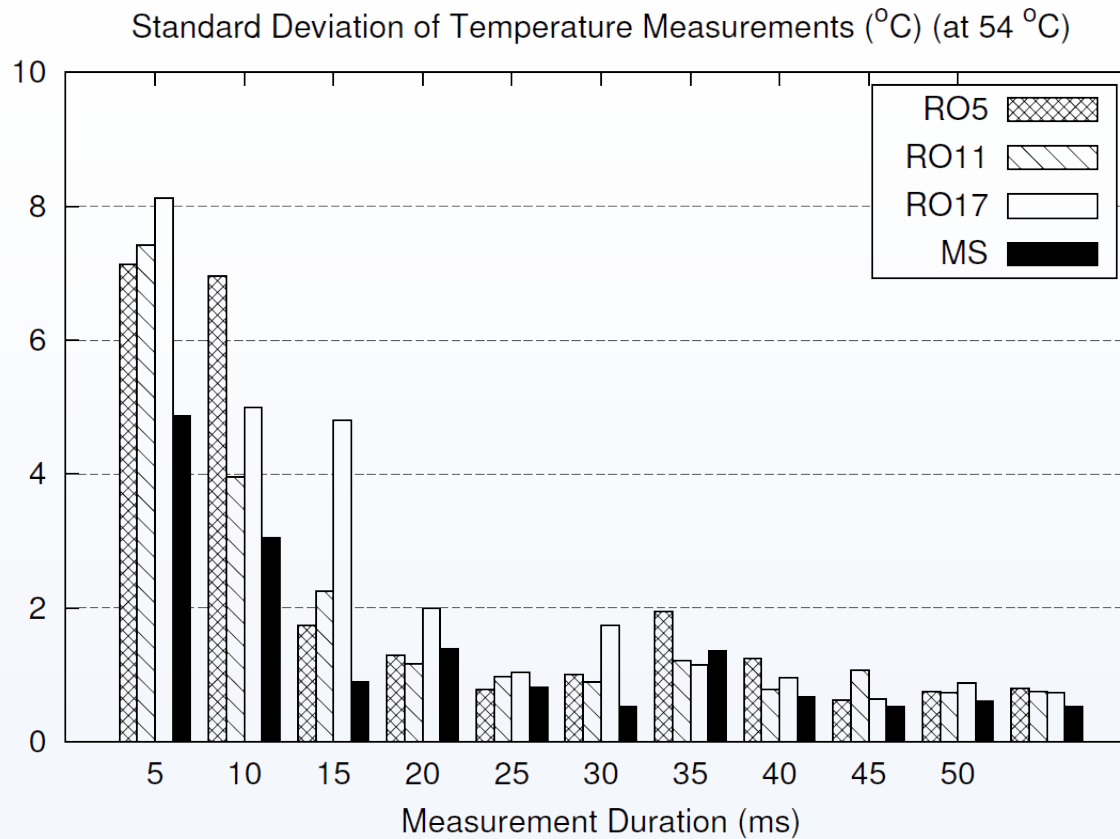
FPGA Measurements

- **Output Response (Voltage):**



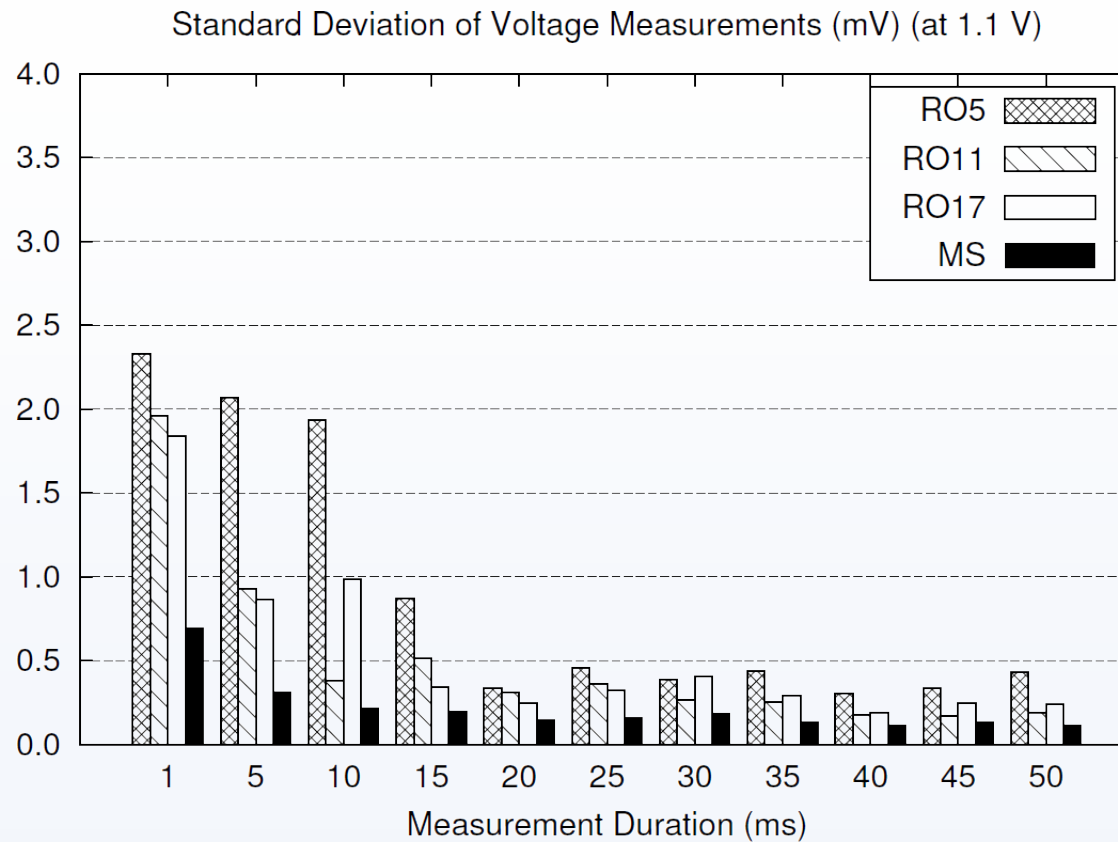
FPGA Measurements

- **Precision (Temperature): 60% average increase**



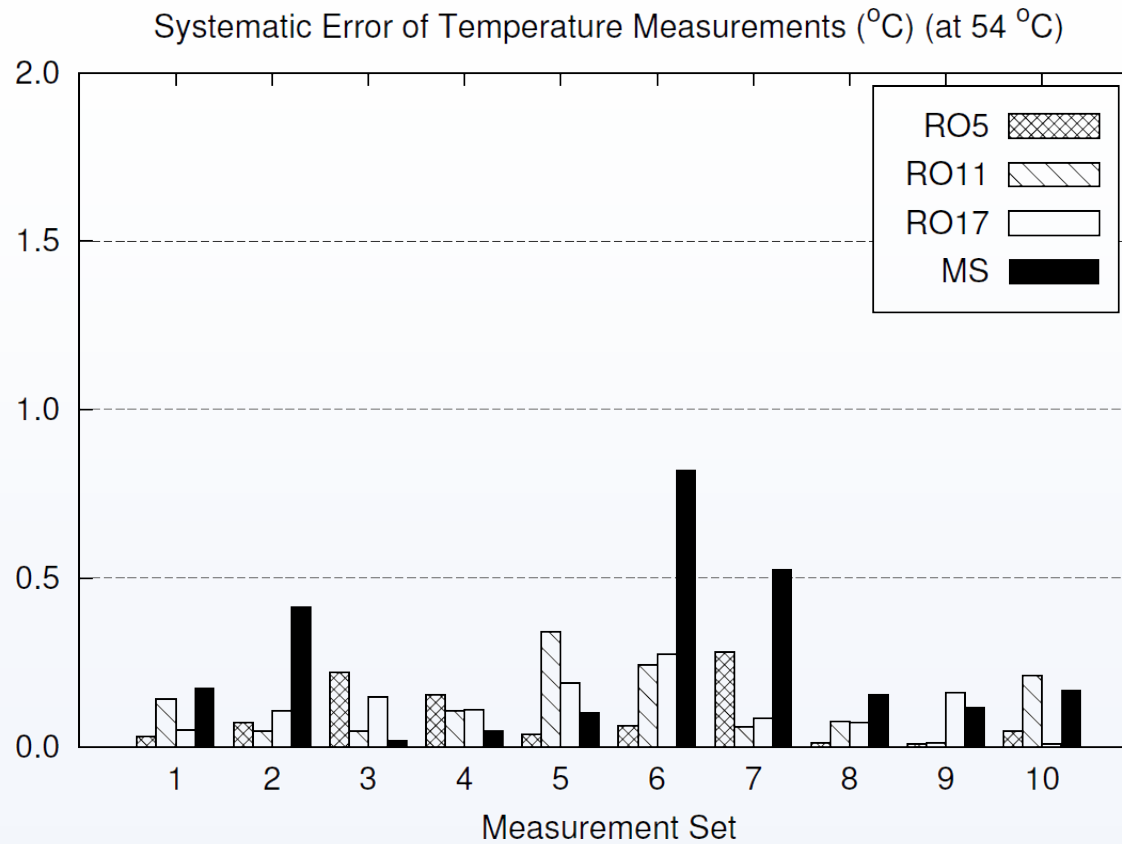
FPGA Measurements

- **Precision (Voltage): 173% average increase**



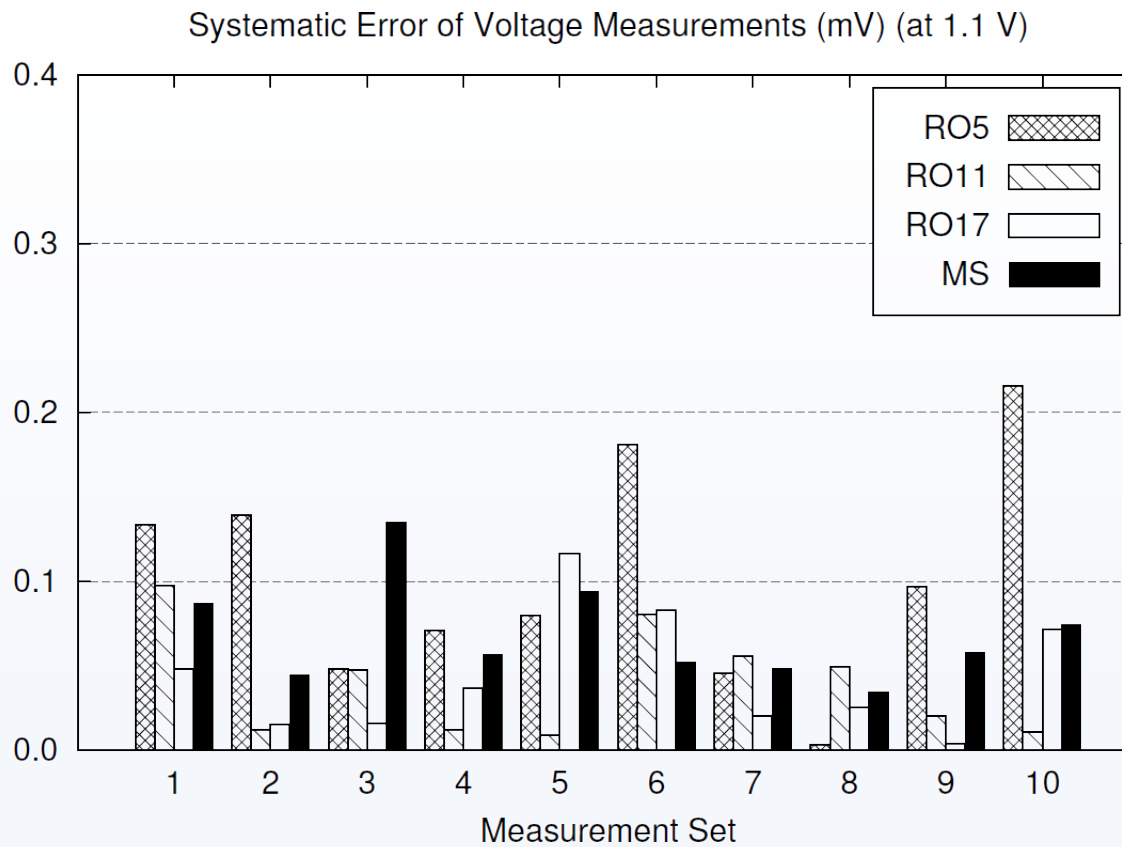
FPGA Measurements

- **Accuracy (Temperature): no significant difference**



FPGA Measurements

- **Accuracy (Voltage): no significant difference**



Conclusion

- Physical parameter sensing supports adaptive, reconfigurable and self-aware applications.
- Presented a novel intra-chip physical parameter sensor based on the phenomenon of flip-flop metastability.
- Proposed design consumes 20% less flip-flops, 75% less LUTs and demonstrated precision improvements of 60% in temperature sensing and 173% in voltage sensing.

End of Presentation