UNIKASSEL VERSITÄT

Area Estimation Of Look-Up Table Based Fixed-Point Computations On The Example Of A Real-Time High Dynamic Range Images System

Michael Kunz, Martin Kumm, Martin Heide, Peter Zipf

In many FPGA-based designs, fixed-point computations can be efficiently implemented by using look-up tables. However, the precision of these computations has a great influence on the hardware costs. We present two simple models for fast but precise area estimation without synthesis, that can be used for word length optimization. As an example, we analyze a LUT-based implementation for high dynamic range (HDR) image processing.

What is the focus of the problem?

- LUT-based realizations of operations and functions are attractive in many cases (like image processing).
- As intermediate values of the computation are non-integer, the (image) quality is significantly affected by rounding errors. These depend on the word length of the values which also affects the hardware complexity.
- Quality measures are needed that accommodate the relation between the required implementation effort and the image quality.

How to be able to estimate the implementation effort in relation to the image quality?

- Other methods rely on pre-synthesized models or analyze the netlist after high level synthesis with a high computational effort for large designs.
- Our method produce an error estimation without high level synthesis.
- The estimation based on two functions — an application specific error metric that specifies the quality of computation and a cost function as a measure of the required implementation effort.
- The estimation itself follows three very simple steps:
  1. Calculation of the error metric in the range of interest,
  2. Calculation of the cost function for these values, and
  3. Building a Pareto front to select the values with the lowest cost and the highest quality.
- Prediction: A design with an appropriate quality can be realized with costs that are below an estimated upper bound.

This is easy! But is this a realistic estimation?

- Example: a LUT-based fixed-point real-time realization of an HDR algo.(Fig. 1.)
- Error metric: mean error of the output pixel compared to its floating point values; Cost function: total bit size of all LUTs.
- Problem: Maximum bit size gives a very pessimistic estimation (worst case model). Including the LUT content and its "minimization potential" into the cost function leads to a more realistic estimation (enhanced model).
- A simple approximation of the real LUT size: cancelling duplicate rows and constant column parts.
- In the enhanced model the relationship is nearly linear, the proposed estimation is very closely related (Fig. 2.).

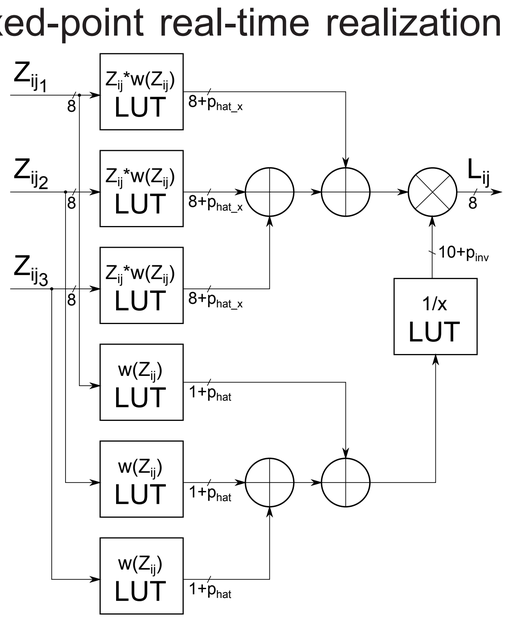

Fig. 1. Block diagram for HDR.

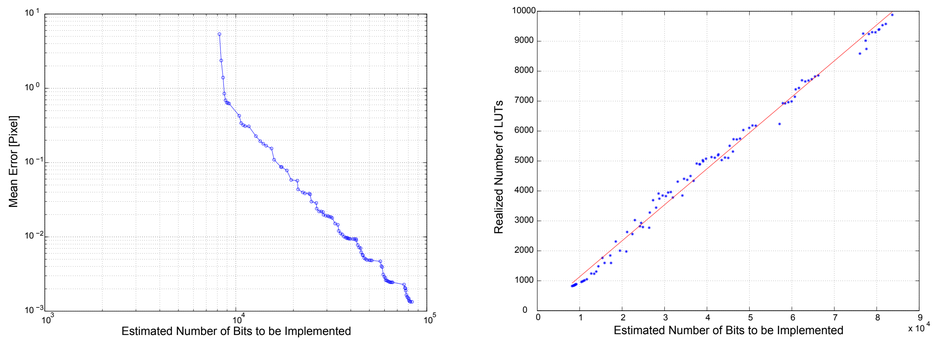

Fig. 2. Enhanced Model: Pareto front (left) and relationship between estimated and realized area (right).