HCM: AN ABSTRACTION LAYER FOR SEAMLESS PROGRAMMING OF DPR FPGA

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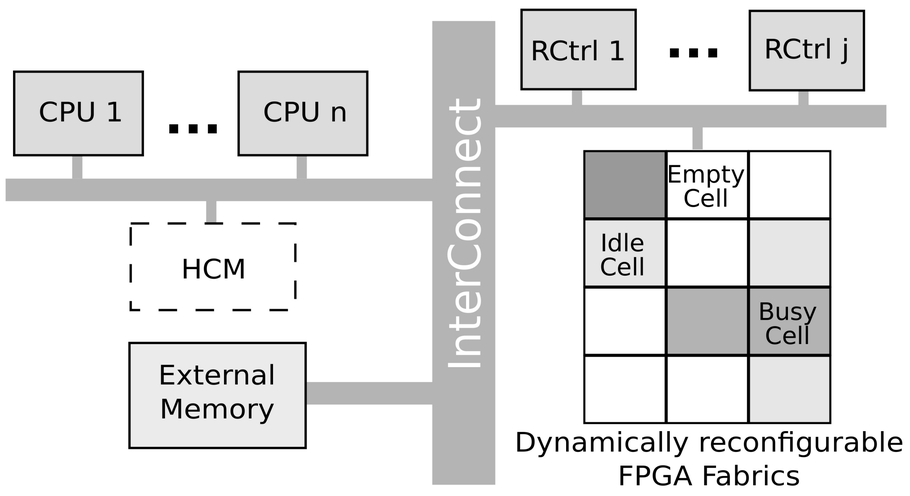
Objectives

For a Dynamic Partial Reconfigurable (DPR) architecture:
- Increasing productivity of application programmer
- Improving flexibility of program
- Solving sharing problem in multi-user context

Approach

- Separating task allocation from FPGA reconfiguration procedure
- Abstracting different kinds of reconfigurable fabrics
- Providing a uniform allocation service to upper layer

Context

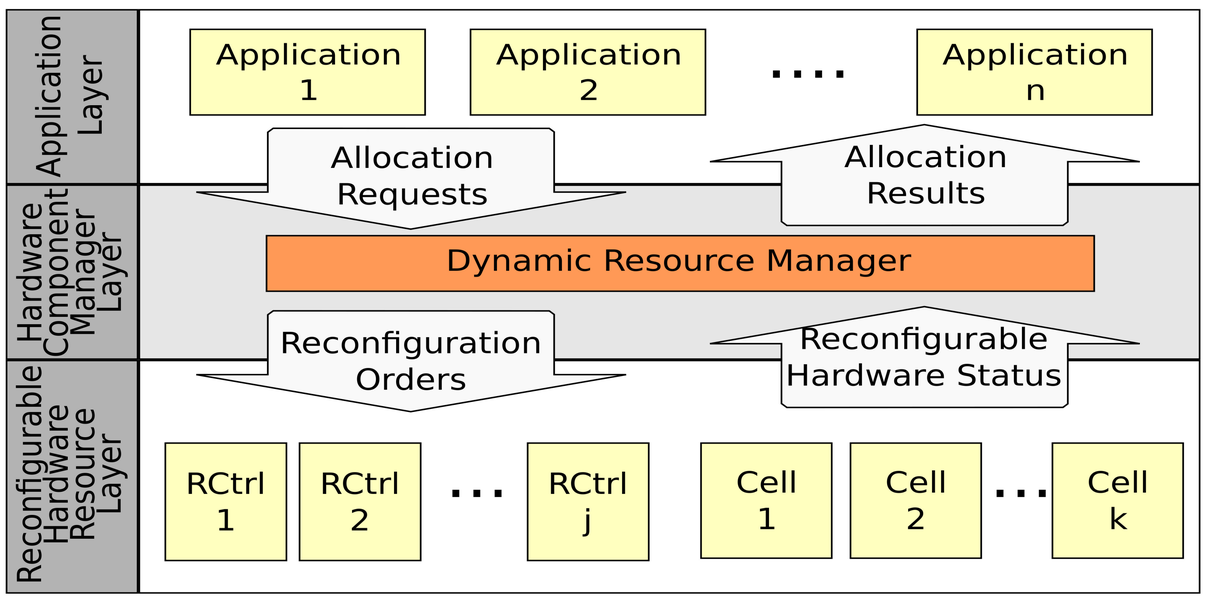


- Cells: homogeneous
- Hardware components: non-preemptive and relocatable

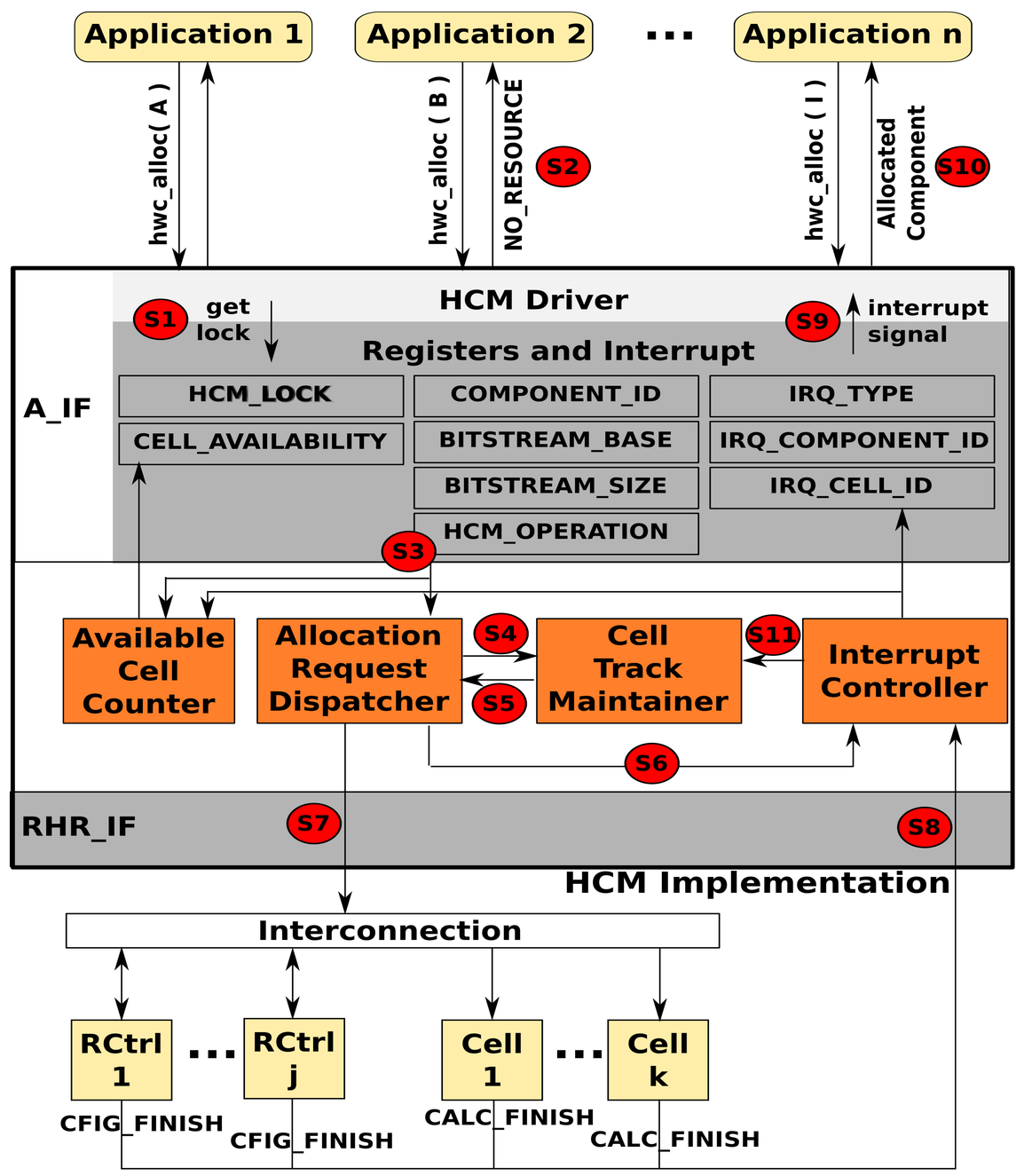
Contribution

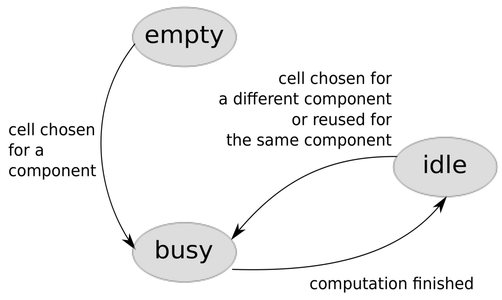
An abstraction layer: **H**ardware **C**omponent **M**anager

- Discharging programmers from reconfiguration control
- Providing protection of cells in multi-user context
- Limiting the number of reconfiguration when possible



HCM Implementation





Three cell states recognized by CTM:

empty - not occupied by any component
busy - being configured or computing
idle - occupied by a component which has finished its computation

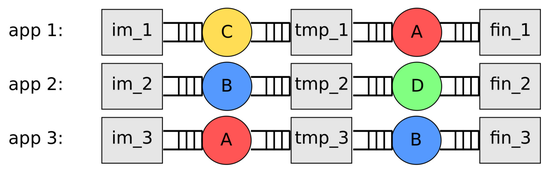
Experiments and Results

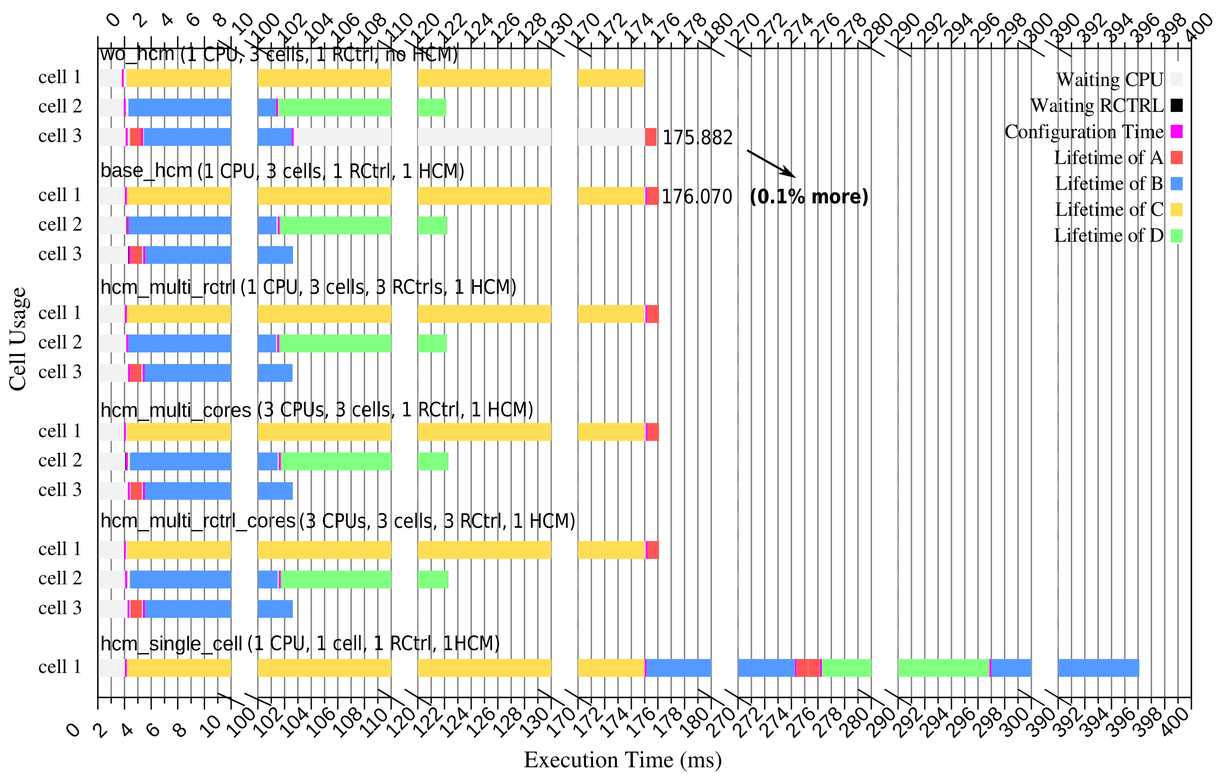
Test Environment:

- Virtual prototype (SocLib/SystemC)
- 6 platforms (5 with HCM, 1 without)
- Different numbers of CPUs, RCtrls and Cells

Applications:

simulated with synthetic workloads.





Results :

- One unique application code for all 5 HCM platforms
- Programmer freed from FPGA reconfiguration control

Conclusion :

- Obvious productivity and flexibiliby gain
- Limited time overhead
- Scaled to multi-CPU, multi-RCtrl context without extra effort