Bitvis

FPGA Development in the Norwegian Industry

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Bitvis AS

- Independent Design Centre for Embedded SW and FPGA (& ASIC)
- Founded January 1, 2012
  - ✓ 6 designers – from March 1, 2012
  - ✓ Expect to increase significantly in 2012/13 (9 designers from Oct.)
- Major focus on Efficiency & Quality Improvement
  - ✓ Through a structured Methodology
  - ✓ Real improvements, - Not just empty words in a company policy…
- Customer partnership
  - ✓ Focus on Customer hand-over (avoiding "legacy consultants")
  - ✓ Also improve customers' methodology (when wanted)
- Methodology, Reviews, Sparring partner

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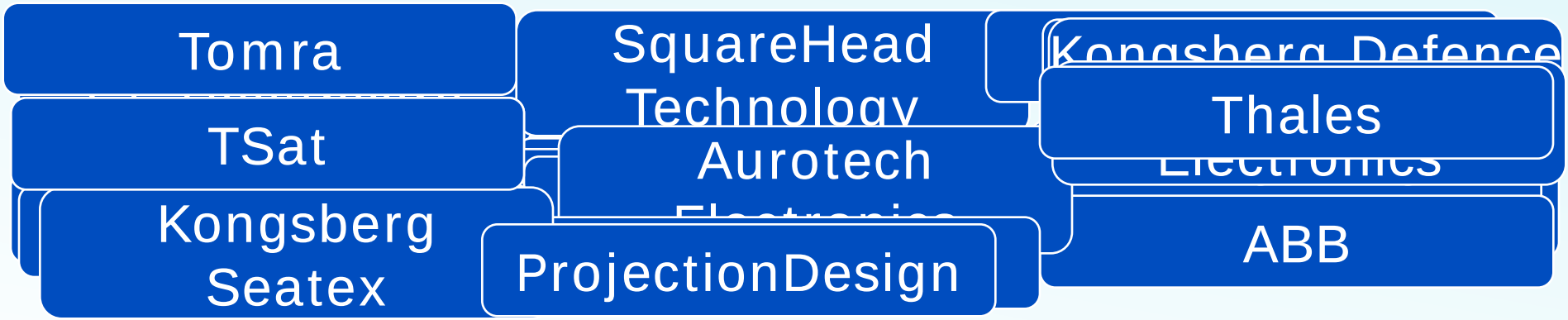
Have you ever heard of it?

Norwegian ASIC/IC Industry

- Chipcon (now TI)
  - ✓ Advanced RF and ZigBee IC solutions (TI 2005, $200M)
- Oracle
  - ✓ World's fastest switches (Infiniband) (for Hi perform. Comp.)
- Falanx (now ARM)
  - ✓ Advanced GPUs (ARM 2006, $30M)
- Atmel
  - ✓ Extremely successful with the AVR (8/32-bit uCtr (Risc))
- Nordic Semiconductor
  - ✓ Ultra low power RF ICs/solutions
- Energy Micro
  - ✓ 'The world's most energy friendly microcontrollers and radios'

Norwegian FPGA projects

- Major diversity
- Succeeding dispite the high level of cost



Cisco

Cisco TelePresence System Codec C90
Originally "Tandberg"
Acquired by Cisco in 2010 ($3,3B)

- 6 FPGA's
- Video composing/scaling and menu overlay of up to 9 full HD (1080p60) outputs
- 15 Gbit/s video backplane over LVDS between FPGA's
- Nios II soft processor
- 280k VHDL code lines (including testbench code)

Cisco PrecisionHD 1080p60 12x Camera

- Complete image processing pipeline in FPGA
- Test-Driven Development (TDD) using custom MATLAB and HDL framework
- Current high-end video conferencing camera
- Image processing pipeline re-used in various Cisco TelePresence Endpoints
- 210k VHDL codelines (including testbench code)

AUROTECH ultrasound

MANUS – Miniaturized Application-Neutral Ultrasound System

- OEM high-end ultrasound engine for medical use.
- Easily and intuitively adapted to customer application.
- Configurable FPGA signal processing is a key to easy meet OEM customer needs.
- Fully parallelized custom signal processing to give high speed of signal processing at low clock rates.
- Example of function implemented in FPGA:
  RX Beamformer 144 GMAC/s @ 125 MHz.
  Input data bandwidth 192 Gbit/s.

Kongsberg Defence & Aerospace

Antifuse to Mercury - BepiColombo mission

15 Feb2012 – Jostein Ekre
Senior System Engineer - Space

KONGSBERG

WORLD CLASS – through people, technology and dedication

BepiColombo mission 2014-2022 to Mercury

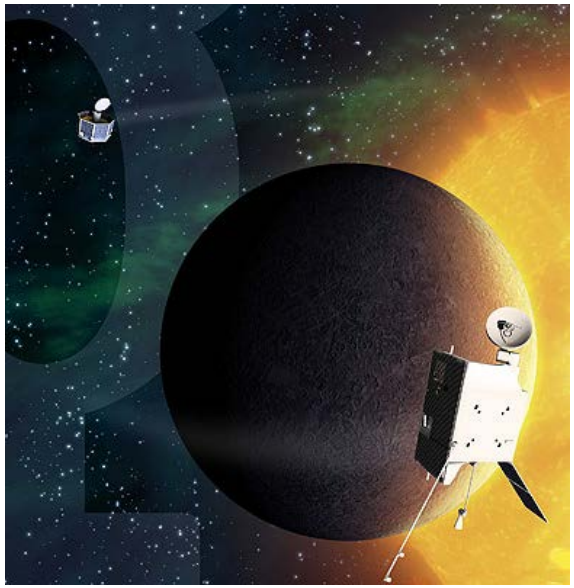
KONGSBERG

- **Journey:** Two orbiters installed on one carrier (MTM) will be launched on a single Ariane 5 rocket from ESA's Spaceport in Kourou, French Guiana in 2014 to Mercury.

- **Transfer module,** Mercury Transfer Module (MTM: 2014-2020)
  - **Kongsberg Defence & Aerospace** is responsible for development and deliverance of SADA(Solar Array Deployment Assembly). KONGSBERG is currently Norway's largest supplier to ESA, the European Space Agency:
  - Earth observation satellites (Aeolus, ENVISAT, GOCE og METOP)
  - Scientific space probes (Cassini-Huygens, Cluster, Darwin, Double Star, Integral, Mars Express, Planck, Rosetta, Soho og Venus Express) -→ BepiColombo
  - Navigation satellites (Galileo)
  - Booster rockets (Ariane 5 DAAV/DAAR, OptoPyro og Vinci)

- **SADA: SADM + SADE**
  - **SADM:** Solar array deployment mechanism
  - **SADE:** Solar Array deployment electronics

- **FPGA related functions in SADA (SADE/SADM):**
  - Commanding the SADM movements through the entire mission from launch to target
  - Control loop Feedback performances
  - Motor torque, current
  - Accuracy of the angular positioning system
  - SADM temperature measurement and accuracy
  - Acceleration and deceleration algorithms
  - Angular Position
  - Housekeeping
  - Timing diagrams of movements and commanded profiles



Norwegian FPGA environment

- Norwegian distribution market is approx the same size as the Swedish distribution market
- A very high relative value of the electronics industry
  - ✓ The utilisation of FPGA technology in the Norwegian electronics industry is very high.
- Lots of really complex FPGAs
  - ✓ Pushing the limits on performance
- Also lots medium complexity FPGAs

FPGA development tend to be time consuming and error prone

→ Must assure the right quality
→ Must constantly improve efficiency

Main quality/efficiency problems

Applies world-wide

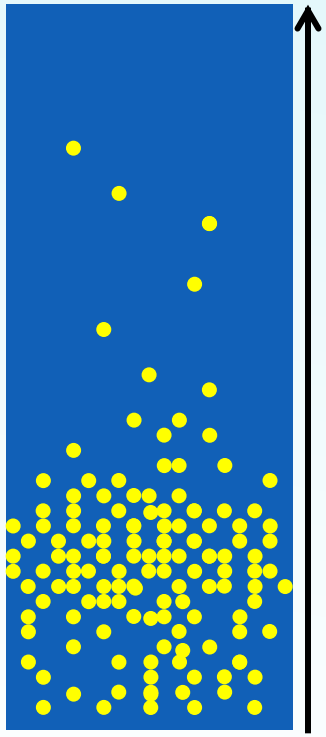
- Most “self inflicted” quality and efficiency problems have the same few root causes.
  - ✓ Design complexity
    - » with lack of structure
  - ✓ Verification
    - » with unstructured TB or lack of simulation
  - ✓ Timing and clocking
    - » Timing Closure
    - » Internal CDC
    - » External I/O timing req. + CDC
- So – what does the FPGA world do about this?

Imbalanced focus on improvement activities

- Tool vendors focus on the most advanced needs
- Academia focus on the most advanced needs

- An advanced focus is required, but…..
- Insufficient focus on the needs of the majority of the industry
  - ✓ Need help – **at the right level**

(Using verification to exemplify…)



Verification – **NOT** the state of the art

- Most companies do not simulate sufficiently
- Most companies have a terrible TB structure
- Most designers have insufficient knowledge about verification and testbenches
- Most companies have insufficient awareness on the importance of proper and structured verification

Verification – what do we need?

- Important to focus on the most advanced needs
  - ✓ For those few who really need it today
  - ✓ For the FPGA community – for the future

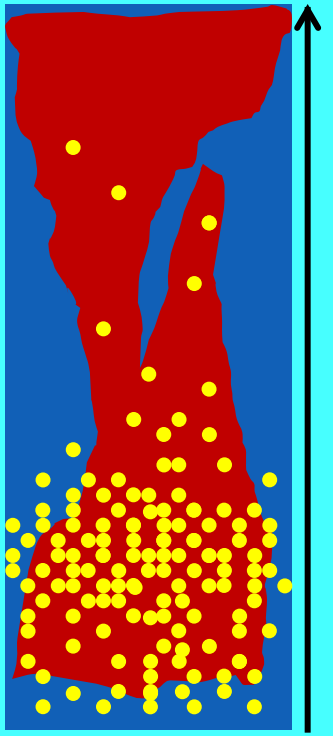
  ➔ Major improvement potential (Quality + Eff.)

BUT:

- The large majority have totally different needs
  - ✓ Awareness → knowledge → experience → structure
  - ✓ Structure: Flow, Documentation, Architecture, Coding
  - ✓ Self-checking, Coverage, Transcripts, Debugging
  - ✓ Step – by – step……
- A huge potential for improvements
  - ✓ For a large majority…
  - ✓ 20-50%

$$$

Verification maturity in companies developing FPGAs



How can we improve verification – for this large majority

- Academia in the education
  - ✓ More on practical approach and structure
  - ✓ More on quality in the development flow
- Academia – research – for the future
  - ✓ Slightly more focus on industry friendly approaches
- Tool vendors
  - ✓ Address the industry at the right level
  - ✓ A company with an insufficient verification methodology first needs help improving awareness, knowledge and structure
    - » THEN they may mature -
      and later become a good customer for advanced solutions….

FPGA Development Best Practices

- Why does this have so little attention
  - ✓ There are courses on technology, languages, frameworks, etc…
  - ✓ But apparently none on FPGA development in general
- Could this be the responsibility of a university…. ?

Bitvis: 2-day course on "FPGA Development Best Practices"

- ✓ A pragmatic and structured approach to handle the main quality and efficiency challenges
- ✓ Focus on the worst time wasters, the most common quality problems and the most important improvement potentials
- ✓ Design structure, Verification structure and CDC
- ✓ Awareness → Knowledge → Practical approach
- ✓ Step – by – step
- ✓ Very good feedback after various courses in Scandinavia

Sharing Knowledge and Experience

- 2004
  - ✓ EMBLA: A Norwegian inter-company cooperation
    - » Intention: High level system development (ASIC + SW)
    - » Byproduct: "Platform based development"
  - ✓ DAK-forum: A 20-year old seminar
    - » Mainly ASIC / Embedded, but also RF, Analog, PCB, FPGA
    - » Exhibition - mainly with the main ASIC tool vendors
    - » Number of participants steadily declining
      - Too academic
      - Too broad
      - Insufficient support from the industry
    - » A very good concept for networking
    - » DAK-forum coordinator very open too new ideas
- 2005 - A joint seminar for DAK-forum & FPGA-forum

FPGA-forum focus

- Main target is the Norwegian Industry
  - ✓ Less academic & less potential future tools/lang/etc.
  - ✓ Narrow focus. FPGA related only
  - ✓ Something of interest throughout the seminar
  - ✓ More presentations relevant to developers' daily work
  - ✓ Minimise direct marketing from the vendors
- 50% of presentations are from the Norwegian industry
  - ✓ On projects, tools, methodology and experience
- Networking
  - ✓ Dinner party gathers >95% of the participants
    - » Important to have the event outside Oslo
  - ✓ Lots of senior developers and decision makers

FPGA-forum today

- Two full days (www.fpga-forum.no)
  - ✓ Two separate tracks
  - ✓ International keynotes (2013: Dennis Segers, CEO Tabula Inc)
    (Previous: Clive Maxfield, Wayne Luk, Patrick Lysaght, Hartenstein, Becker)
- 120-130 participants

Next FPGA-forum:
Wedn+Thur, February 13-14, 2013 (in Trondheim)

- Exhibition and Recruitment stand
  - ✓ All the major Vendors are present
  - ✓ Vendors very pleased with "the quality of the participants"
- High quality presentations
  - ✓ Very good feedback from the partcipants
- Helps the Norwegian FPGA community improving

Summary

- There **is** an electronics industry in Norway
  - ✓ Part of the FPGA industry is really advanced
  - ✓ The cost of living is not a show stopper
  - ✓ Engineers and specialists are **relatively** cheap
- Imbalanced focus from vendors and academia – world-wide
  - ✓ Need more Awareness, Knowledge, Structure & Reuse
  - ✓ Best Practices and good structuring may reduce workload by 20-50% - with improved quality as a bonus
- FPGA-forum contributes to a better FPGA community
  - ✓ Focusing on the needs of the industry is critical
  - ✓ There are of course lots of improvement potentials…

Thank you

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