CRUSH: Cognitive Radio Universal Software Hardware

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State of the Art in Software Defined Radio

+ Attach agile radio frequency front end to host computer to perform radio functions using software such as GNURadio or Matlab

+ More flexible than fixed hardware systems; all network layers can be implemented and modified in software

- Software adds latency and decreases system speed; data must be transferred between host and front end, not designed for real time operation

CRUSH is real-time capable and moves processing closer to the RF receiver/transmitter
Goals of CRUSH

+ Use FPGAs in SDR front ends, treating the hardware description language (HDL) as “software”

+ Process data close to the receiver/transmitter. Remove latency.

+ Existing SDR platforms (Ettus USRP, WARP from Rice University) have onboard, user modifiable FPGAs
  - Modifying existing HDL can be complex
  - RF components and FPGA integrated on a single board
  - FPGAs and RF front ends are released on different schedules

CRUSH decouples fast evolving FPGA hardware from the RF front end
Outline

• SDR overview and motivation

• Hardware Platform
  – Cognitive Radio Universal Software Hardware (CRUSH)

• Cognitive radio overview

• Application: Spectrum sensing

• Results

• Summary
CRUSH Components

- **Hardware**
  - Xilinx ML605 FPGA Development Board
  - Ettus Research USRP N210
  - Custom Interface Board

- **Hardware Description Language (HDL) Framework**
  - USRP HDL modified for CRUSH
  - ML605 HDL created from scratch for CRUSH

- **Software**
  - Discussed later in presentation
Ettus USRP N210

Universal Software Radio Peripheral
- Designed by Ettus Research
- Utilizes Xilinx Spartan 3A DSP series FPGA
- Popular academic SDR platform
- FPGA mostly filled with existing radio functionality
- USRP used as RF front end for SDR implemented in either GNUradio or Matlab
- CRUSH uses USRP N210 coupled with a high end FPGA board for SDR
Introducing CRUSH

Cognitive Radio Universal Software Hardware (CRUSH)

- Standard software defined radio and FPGA development board
- Custom interface board to connect the two boards

Xilinx ML605 FPGA Board

Ettus USRP N210

Custom Interface Board
Xilinx ML605 FPGA Development Board

Specifications:
- Xilinx V6-LX240t FPGA
- 1* high pin count FMC
- 1* low pin count FMC
- 1* PCI express 8 x
- 512 MB DDR3 RAM

Benefits:
- Standard FPGA development board
- Ability to communicate at full ADC and DAC rate with the USRP
- Versatile external I/O/memory
- Increases from USRP FPGA: 6.6 × more RAM, 4.5 × more LUTs, 2.5 × faster
Custom Interface Board

- 2 Micror connectors
  - Allows for ML605 to communicate with two USRPs via the 34 pin parallel debug port
- 2 miniSAS posts
  - Transmit serial data with up to two USRPs via MIMO port
- 2 spare Micror connectors
  - Spare FPGA IO
- FMC HPC/LPC interface
  - Fully compatible with the ML605
  - Can be used with and LPC interface like the SP605 with just one USRP
- Only custom part of CRUSH
- Allows full 100 MSPS IQ bidirectional datalink up to 800 MB/s
USRP HDL Framework

Acronyms:
• ADC – Analog to Digital Converter
• DDR – Double Data Rate
• NCO – Numerically Controlled Oscillator
• MUX – Multiplexer

Legend:
- USRP
- CRUSH
- HOST

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ML605 HDL Framework

Acronyms:
- LUT – Look Up Table

Legend:
- USRP
- CRUSH
- HOST

Framework takes up just 3% of Logic, 97% Free for User Block
Outline

- SDR overview and motivation
- Hardware Platform
- Cognitive radio overview
- Application: Spectrum sensing
- Results
- Summary
Cognitive radios allow you to operate in unused portions of spectrum
• Existing Software Defined Radio (SDR) systems take too long to perform spectrum sensing
• Software spectrum sensing involves transmitting data to and from the host computer which adds latency and processing time
• Moving spectrum sensing closer to the receiver reduces latency and makes real time spectrum sensing feasible
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Spectrum Sensing – Energy Detection

1. Receive RF Data
2. Perform FFT
3. Apply Threshold
4. Report Data
System Diagram – Without CRUSH

- All processing occurs on the host
- No real-time guarantee
Acronyms:
- FIFO – First In First Out
- FFT – Fast Fourier Transform

Legend:
- USRP
- CRUSH
- HOST

Digital Down Converter (DDC) → ADC → Radio
Digital Up Converter (DUC) → Transmitter
DAC Data → Receiver

Frequency Selection

Host Control Logic

FIFO → FFT → Threshold Detector

ML605 Control Logic
User Block

- Xilinx FFT
  - 8-4k point size
  - Streaming
  - Scalable
- I and Q Magnitude
- Thresholding
  - User specified
- Result Storage
  - FFT
  - Threshold
Advantages

• Ability to process received data in real time
  – FPGA: Parallel clock driven data bus
  – Host: Serial packetized data

• Higher throughput datalink
  – FPGA: 100 MHz 32 bit DDR interface (800 MB/s)
  – Host: Gigabit Ethernet (125 MB/s)

• Less processing load on the host
  – More time for high level policy / protocol execution

• Reconfigure hardware allows for parameters such as FFT size to be changed in real time

• New protocols with functionality partly residing on the host and partly on the radio are now possible
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Results Breakdown

• Test Setup
  – CRUSH Software
  – CRUSH Equipment Configuration

• Functional Verification
  – Prove the functionality of the FFT used for Spectrum Sensing
  – Visually show a comparison of USRP and CRUSH

• FFT Timing
  – Show modifications needed for precise timing
  – Look at a 256-point example in detail
  – Compare the time for completion of an FFT on both CRUSH and the USRP

• End to End CRUSH Timing
  – Show modifications needed for timing on the host
  – Look at the end to end timing of CRUSH measured by the host

• Real World Examples
  – CRUSH Matlab Demo
  – Free Space Spectrum Sensing
Test Setup - Software

USRP Hardware Driver (UHD) C++ Code:
+ Fast
+ Integrated in GNURadio
+ Ability to also control USRP
+ Fully configurable
- No graphical support
- Not user friendly

Matlab Spectrum Sensing Demo:
+ Quickly demonstrate CRUSH
+ Dynamically vary parameters
+ Manual or automatic updates
+ Graphs data for quick analysis
- Not real time (ms vs us)
- This demo not integrated into SDR

Debug Serial Port:
+ Debug Interface
+ Access more detailed settings
+ Contains all functions of UHD
+ Reprogrammable in software
- Slow
- Not user friendly
Test Setup – Equipment Configuration

Signal Generator -> USRP -> ML605 -> Host
Results – Functional Verification

- Data recorded via USRP software
- 73 MHz CW tone
- 70 MHz Center Frequency
- 256-point FFT, 25 MHz Bandwidth
- USRP Data is filtered and Decimated by the dsp_core block

- Data sent over Ethernet using CRUSH and recorded using Matlab
- 1024-point FFT, 100 MHz Bandwidth, 25 MHz shown to match USRP
- Verifies FFT in CRUSH
FFT Timing – Required Modifications

- Added Timers to ML605 and special control logic to the USRP
FFT Timing – Detailed Steps

1. Host -> ML605 (start test)
2. ML605 (reset timers)
3. ML605 -> USRP (start test)
4. USRP -> Host / ML605 (test pattern)
5. USRP / ML605 Processing
6. ML605 FFT Done (stops timer)
7. Host -> ML605 (FFT Done)
8. Host FFT Done (stops timer)
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8. Host FFT Done (stops timer)
256-point FFT Example

- FFT Starts on first word, streams thereafter
### Results – FFT Timing Analysis

<table>
<thead>
<tr>
<th>FFT Size</th>
<th>FPGA Average (μs)</th>
<th>Host Average (μs)</th>
<th>Speed-up (x)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>1.17</td>
<td>907.72</td>
<td>774</td>
</tr>
<tr>
<td>16</td>
<td>1.91</td>
<td>915.89</td>
<td>479</td>
</tr>
<tr>
<td>32</td>
<td>2.38</td>
<td>920.07</td>
<td>386</td>
</tr>
<tr>
<td>64</td>
<td>3.56</td>
<td>925.47</td>
<td>259</td>
</tr>
<tr>
<td>128</td>
<td>5.47</td>
<td>916.54</td>
<td>167</td>
</tr>
<tr>
<td>256</td>
<td>9.56</td>
<td>1198.19</td>
<td>125</td>
</tr>
<tr>
<td>512</td>
<td>17.23</td>
<td>1003.83</td>
<td>58</td>
</tr>
<tr>
<td>1024</td>
<td>32.84</td>
<td>955.30</td>
<td>29</td>
</tr>
<tr>
<td>2048</td>
<td>63.55</td>
<td>995.26</td>
<td>15</td>
</tr>
<tr>
<td>4096</td>
<td>125.24</td>
<td>1071.79</td>
<td>8</td>
</tr>
</tbody>
</table>

- Speed-up between 8 and 774 \(x\)
- FPGA timing scales log linear with FFT size
- Host timing driven by packet transmit time and internal buffering
Results – FFT Runtime

Host vs ML605 FFT Runtime

FFT Size

Time (µs)

CRUSH
Host
± Standard Deviation

FFT Size
• Moved timer into the host, allows for end to end timing analysis
• Measured and recorded through the UHD C++ Code
Results - End-to-end Timing

Roundtrip Time for CRUSH FFT Completion

Time [us]

CRUSH FFT
CRUSH Roundtrip
Host
± Standard Deviation

FFT Size

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Real World Example: Free Space Test

- Free space test @ 915 MHz – 1W transmitter in ISM band
Real World Example: Matlab Demo

- **Blue** represents the FFT values from CRUSH
- **Red** represents the threshold values
- **Green** is the threshold

- Parameters adjustable on bottom of demo
- Left side is a Magnitude plot
- Right side is a dB plot
Conclusion

- Created CRUSH platform
  - Combined powerful FPGA with versatile RF front end
  - Produced custom interface board to allow high speed data transfer
  - Moved processing closer to the receiver
  - Decoupled the fast evolving FPGA platform from the custom RF front end

- Implemented spectrum sensing on CRUSH
  - Achieved more than 100x performance for FFT on point sizes of interest
  - Roundtrip timing beats USRP by 10x
  - Reduced load on host computer
  - Fully configurable
Future Work

- Integrate the spectrum sensing module into research on Cognitive Radio at Northeastern University
- Explore other methods of performing hardware accelerated spectrum sensing such as wavelet analysis
- Utilize the CRUSH platform to migrate additional software radio functions into reconfigurable hardware
- Perform non-radio research with the CRUSH platform utilizing its RF front end and FPGA back end
CRUSH software and users manual will be available from September at

http://www.coe.neu.edu/Research/rcl//projects/CRUSH.php

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Backup Slides
Wireless Open-Access Research Platform

- Designed by Rice University
- Latest uses Xilinx Virtex 4 FX FPGA
- 4 daughterboard slots for ADC, DAC or IO
- More processing power than USRP but the hardware is becoming dated
- Design is based on FX series FPGA which has been discontinued
- CRUSH decouples the FPGA from the RF portion and reduces the effect of old hardware

*http://warp.rice.edu/trac/*
Related Work - GNURadio

• Both a Visual (GNURadio Companion) and programming (python) environment for SDR implementations
• Fully supports the USRP and other common SDR RF front ends
• Backend of GNURadio is highly optimized C libraries and front end is python scripts to connect the C libraries together
• Users can quickly get the system up and running and observe spectrum via FFTs, send simple data and implement radio protocols
• http://gnuradio.org/redmine/projects/gnuradio/wiki
Results – End to End CRUSH Timing

Roundtrip Time for CRUSH FFT Completion

<table>
<thead>
<tr>
<th>FFT Size (bytes)</th>
<th>Average Time [us]</th>
<th>Standard Deviation</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>110</td>
<td>10</td>
</tr>
<tr>
<td>16</td>
<td>115</td>
<td>12</td>
</tr>
<tr>
<td>32</td>
<td>120</td>
<td>15</td>
</tr>
<tr>
<td>64</td>
<td>125</td>
<td>18</td>
</tr>
<tr>
<td>128</td>
<td>130</td>
<td>20</td>
</tr>
<tr>
<td>256</td>
<td>135</td>
<td>22</td>
</tr>
<tr>
<td>512</td>
<td>140</td>
<td>25</td>
</tr>
<tr>
<td>1k</td>
<td>145</td>
<td>28</td>
</tr>
<tr>
<td>2k</td>
<td>150</td>
<td>30</td>
</tr>
<tr>
<td>4k</td>
<td>155</td>
<td>32</td>
</tr>
</tbody>
</table>

Time in microseconds (us) vs. FFT Size.
Serial Debug Port

ML605 to USRP V0.8
George Eichinger

Firmware ID: 0x55535250
Firmware Version: 0x40001

Please select an option:
1: start test - internal data
f: start test - fifoed data
t: start test - raw data
F: start test - filtered data
O: start test - output of FFT
v: print firmware version
L: light 4 LEDs using binary aka [>>L 0101]
d: print dip status
s: set the desired remote frequency 0-100M [>>s 005]
h: set threshold [>>h 05]
w: set transform log2 width [>>r 09 = 2^9=512]
m: set mode [>>m 0]
1: set mode new [>>1 0]
2: set the desired remote frequency new 0-100M [>>2 005]
3: set echo in hex [>>3 deadbeef OR >>3 0101ababe]
4: set transform log2 width [>>4 09 = 2^9=512]
5: start test - raw data
6: set FFT scale [>>6 43691 or >>6 00156]
7: send test packet
8: start test - thresholded
9: set the threshold {>>9 12345678}
u: run double test, fft & thresh