Using DSP Block Pre-adders in Pipeline SDF FFT Implementation in Contemporary FPGAs

Carl Ingemarsson, Petter Källström and Oscar Gustafsson
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DFTs are widely used in, e.g., OFDM communications.
Straight forward implementation of FFT is common.
This implementation is not efficient in FPGAs.
We have mainly focused on the 6 and 7 series Xilinx FPGAs.
Radix-2 SDF FFT Structure

Entire structure of a 64 point radix-2 SDF FFT processor.
One stage

Original structure of one stage of the FFT architecture.
First Optimization

Key transformation relation: \( X = \frac{X + X}{2} \).
Utilizing the existing pre-adder in the DSP-blocks.
If the pre-adder has a bypass function, this allows a third transformation, affecting the content in the shift register.
## Optimization Summary

Resource usage with respect to word length $W$.

<table>
<thead>
<tr>
<th></th>
<th># LUTs</th>
<th># DSP48s</th>
</tr>
</thead>
<tbody>
<tr>
<td>Original</td>
<td>$W \times 6$</td>
<td>4</td>
</tr>
<tr>
<td>Optimization 1</td>
<td>$W \times 4$</td>
<td>4</td>
</tr>
<tr>
<td>Optimization 2</td>
<td>$W \times 3$</td>
<td>4</td>
</tr>
<tr>
<td>Optimization 3</td>
<td>$W \times 2$</td>
<td>4</td>
</tr>
</tbody>
</table>

One extra bit in each adder, used for sign extension, is required, using one LUT each (4, 4, 2, 2 in the designs, respectively).
## Implementation Results

Implementation results for 16 bit word length in a Xilinx Virtex 6 (xc6vsx315t).

<table>
<thead>
<tr>
<th></th>
<th># slices</th>
<th># LUTs</th>
<th># DSP48E1s</th>
<th>Expected</th>
</tr>
</thead>
<tbody>
<tr>
<td>Original</td>
<td>44</td>
<td>116</td>
<td>4</td>
<td>(16 \cdot 6 + 4 = 100)</td>
</tr>
<tr>
<td>Opt. 1</td>
<td>20</td>
<td>68</td>
<td>4</td>
<td>(16 \cdot 4 + 4 = 68)</td>
</tr>
<tr>
<td>Opt. 2</td>
<td>21</td>
<td>50</td>
<td>4</td>
<td>(16 \cdot 3 + 2 = 50)</td>
</tr>
<tr>
<td>Opt. 3(^1)</td>
<td>10</td>
<td>34</td>
<td>4</td>
<td>(16 \cdot 2 + 2 = 34)</td>
</tr>
</tbody>
</table>

\(^1\) Manual placement required.

Expected number of LUTs includes sign extension in additions.
**Applicability to Other FPGAs**

- Optimization 1 can be applied to most FPGAs.
- Optimization 2 utilizes the pre-adder of contemporary FPGAs.
- Optimization 3 needs a pre-adder with bypass functionality.
Conclusion

- We have proposed transformations of a radix-2 SDF stage.
- These transformations reduce the LUT usage and utilize pre-adders of the DSP blocks.
- This is applicable to Xilinx’ 6 and 7 series FPGAs, but should be usable also in other FPGA families.
Thank you.

Any questions?