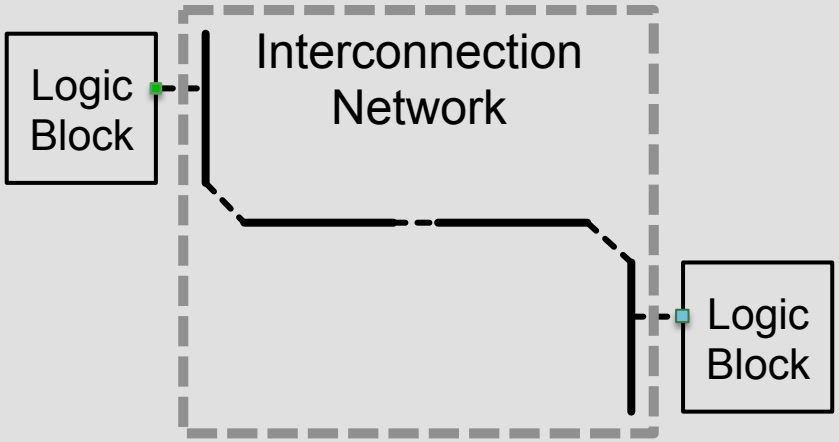
On the Difficulty of Pin-to-Wire Routing in FPGAs

Niyati Shah
Department of ECE
University of Toronto
shahniya@eecg.utoronto.ca

Jonathan Rose
Department of ECE
University of Toronto
jayar@eecg.utoronto.ca

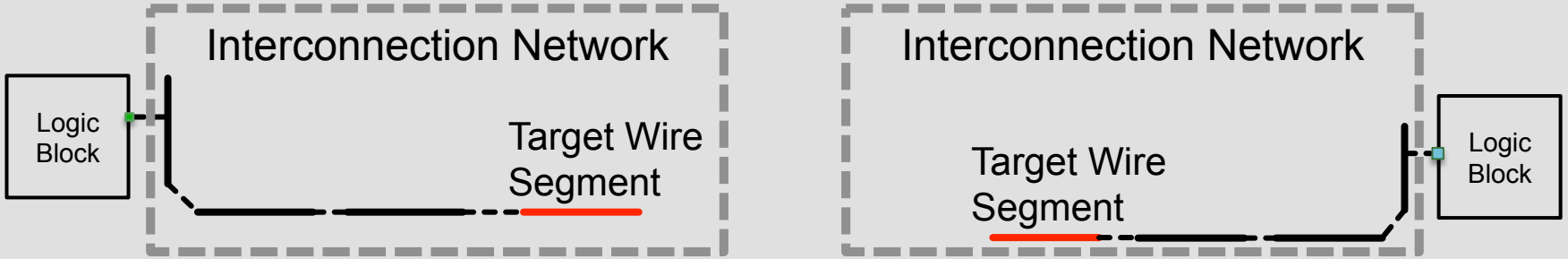
Traditional Pin-to-Pin Routing

- Involves connecting output pins of logic blocks to input pins of other logic blocks
- Interconnection network is designed by an FPGA architect to achieve routability when connecting pins to pins



Unusual: Pin-to-Wire Routing

- Making connections from output pins of logic blocks to specific "target" wire segments in the FPGA
- Or from specific wire segments to input pins



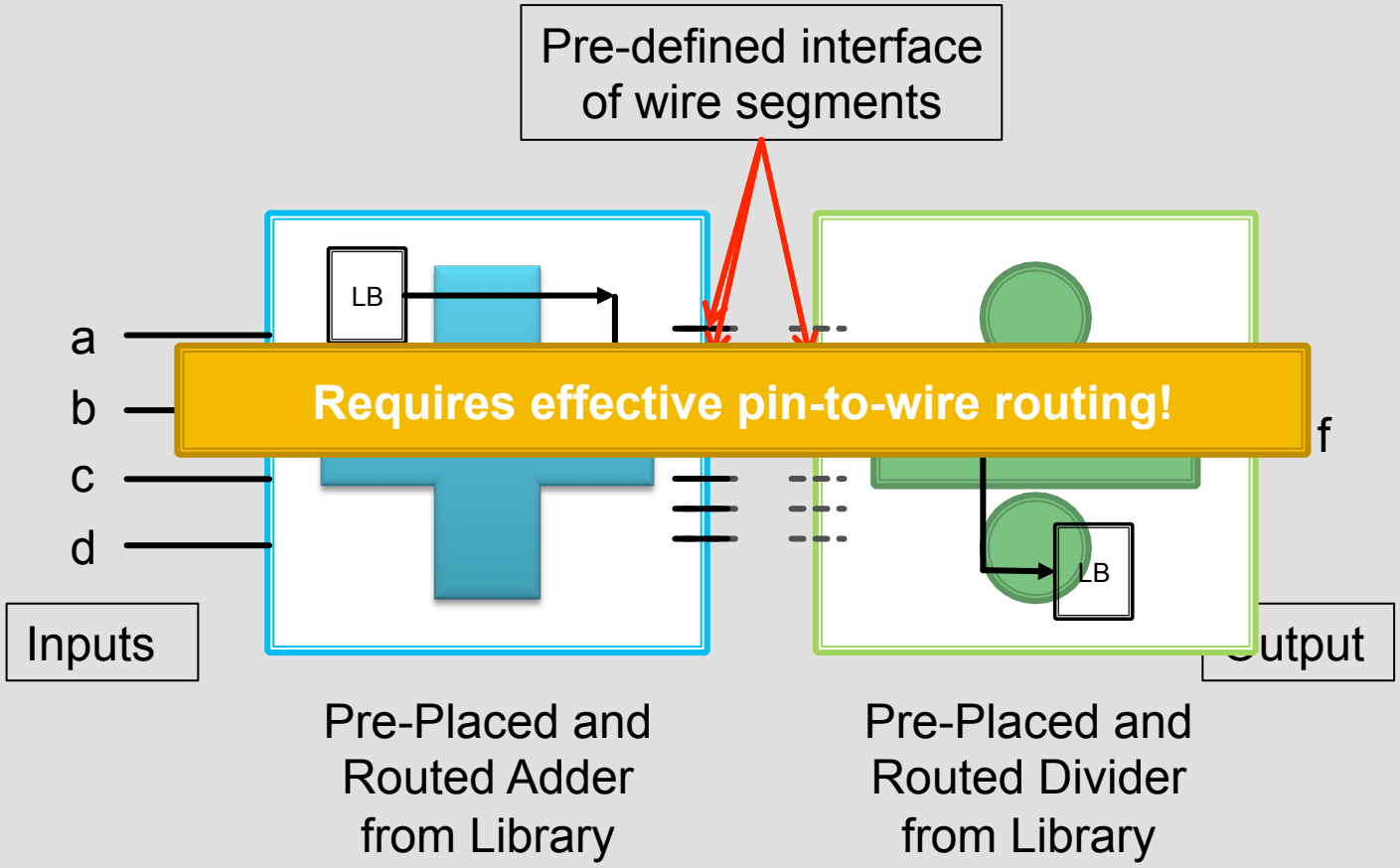
Motivation:
Why Pin-To-Wire Routing?

Motivation 1: Routing by Abutment

- Modern FPGAs are so large, and with processor speed no longer scaling, compile time is a huge issue
- One Solution: pre-compiled blocks that route by abutment

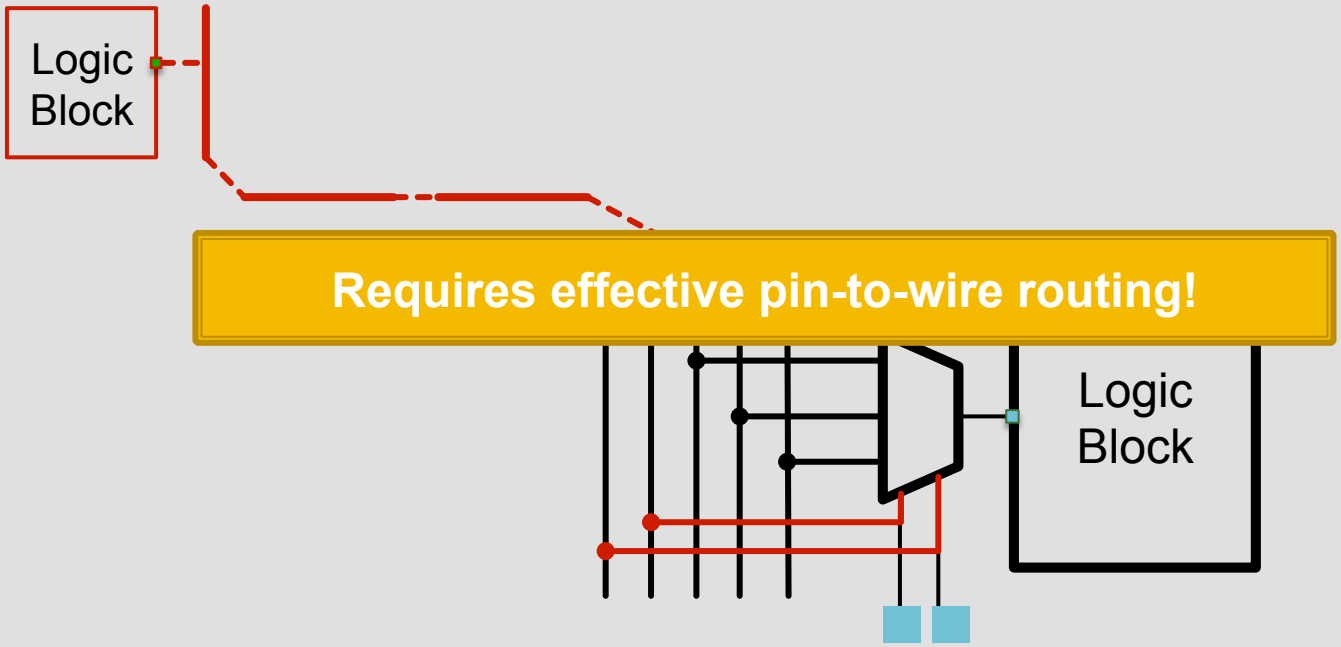
Routing By Abutment Illustrated

$f=(a+b+c)\div d$



Motivation 2: Using FPGA Routing Circuit Elements

- Multiplexers: Expensive to implement in soft logic; plenty in the fabric. Why not use ‘em as logic?



Using an Input Connection Block Multiplexer as a Logic Multiplexer

There is a Problem with P-to-W

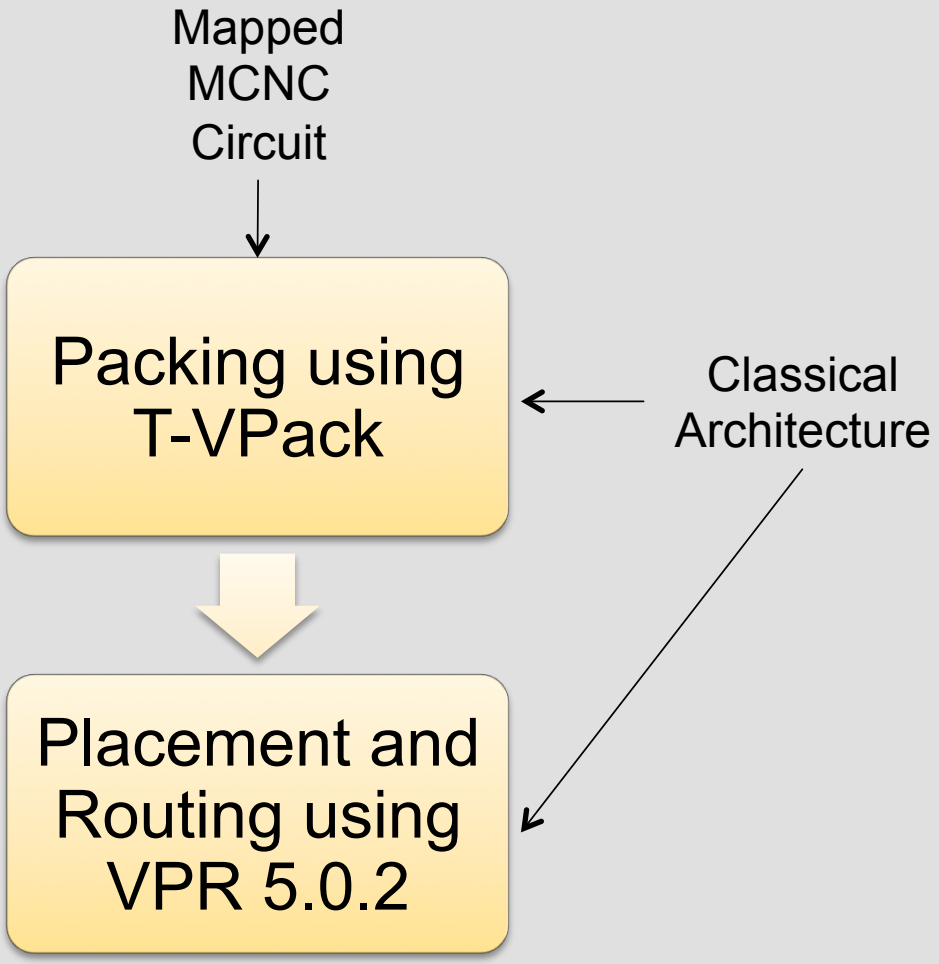
- Effective Pin-to-Wire Routing conflicts with the basic purpose of FPGA routing architectures:
  - Efficiently enable **Pin-to-Pin** Routing
- Pin-to-Wire routing missing one interconnect stage
  - The final or initial connection block
- Many ways to enter and exit a logic block but limited ways to enter and exit a wire segment
- Clearly, Pin-to-Wire Routing will be more difficult

Goal: Measure how Difficult

- Difficult, but not impossible
  - Most FPGAs are architected to ensure that circuits with high routing demand will succeed
    - Not all circuits have high demand
- Hypothesis: For some circuits the extra routability could make up for difficulty of Pin-to-Wire Routing
- Will test hypothesis experimentally and measure impact of Pin-to-Wire routing on
  1. Routed wirelength,
  2. Critical path delay
  3. Router effort (router heap push and pop count)

Experimental Methodology

Design Flow


Mapped
MCNC
Circuit
Packing using
T-VPack
Classical
Architecture
Placement and
Routing using
VPR 5.0.2

Experiment Design and Results

Abutment-Like Pin-to-Wire Routing

Method is proxy for routing-by-abutment motivation:

For each circuit:

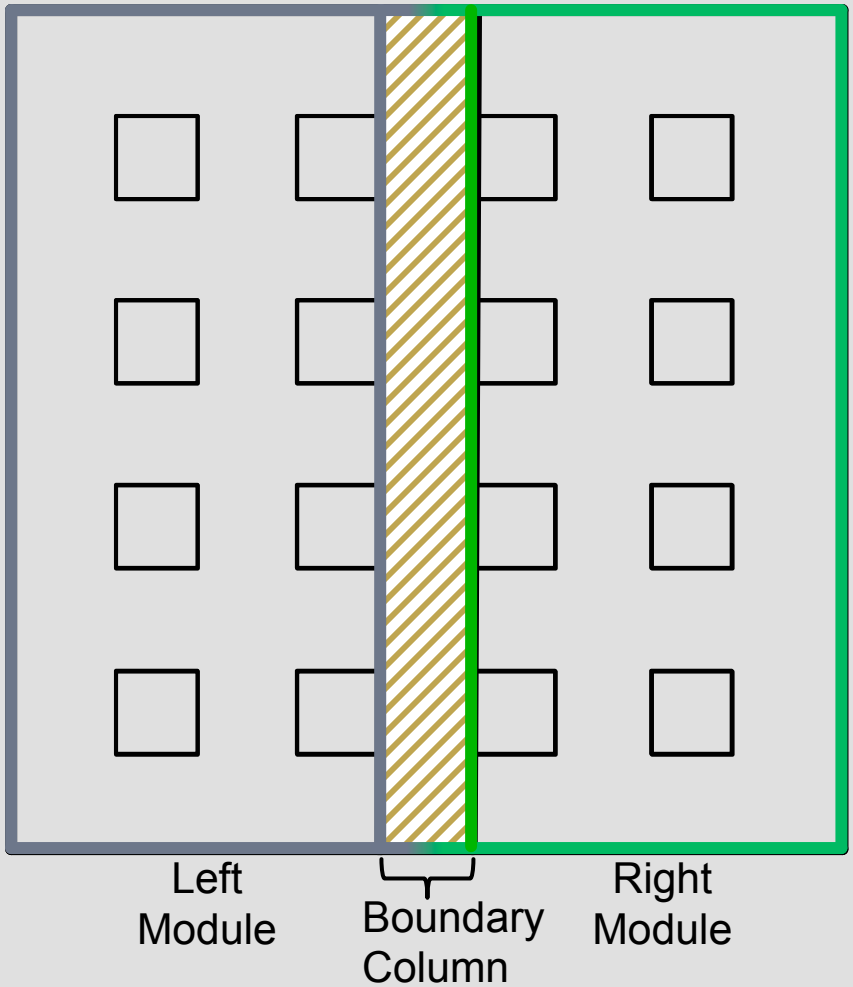
1. Run regular flow: pack, place & route
2. Determine minimum tracks per channel, **W**
3. Set tracks to **W**+30%

Call this '**Base Routing'** and record:

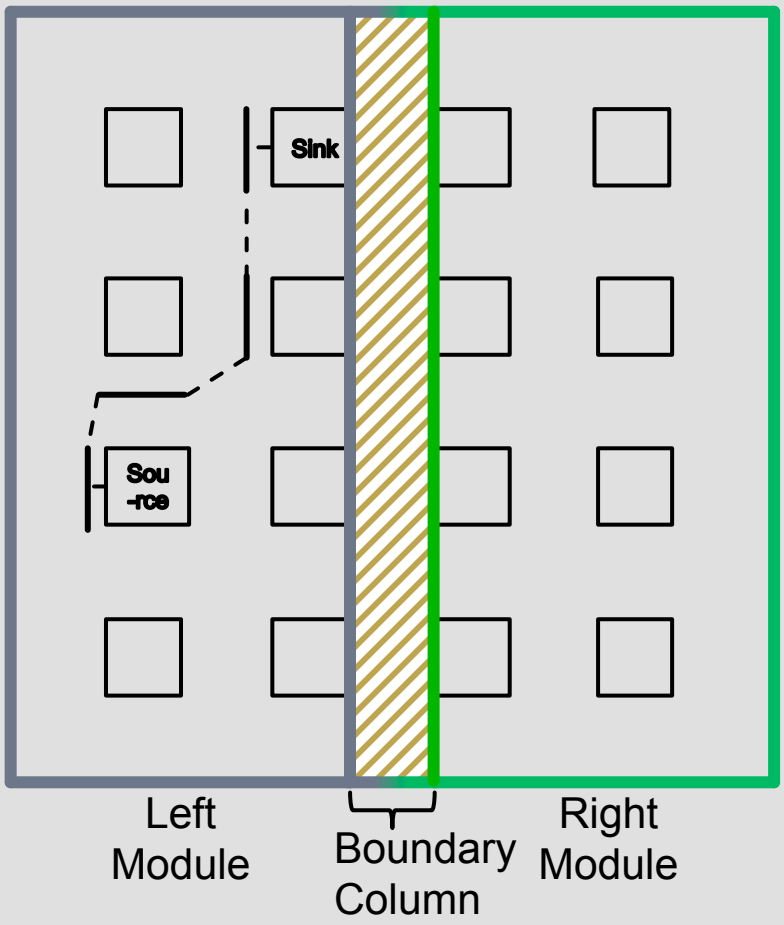
1. Routed wirelength,
2. Critical path delay
3. Router effort

Then: Divide the FPGA in half

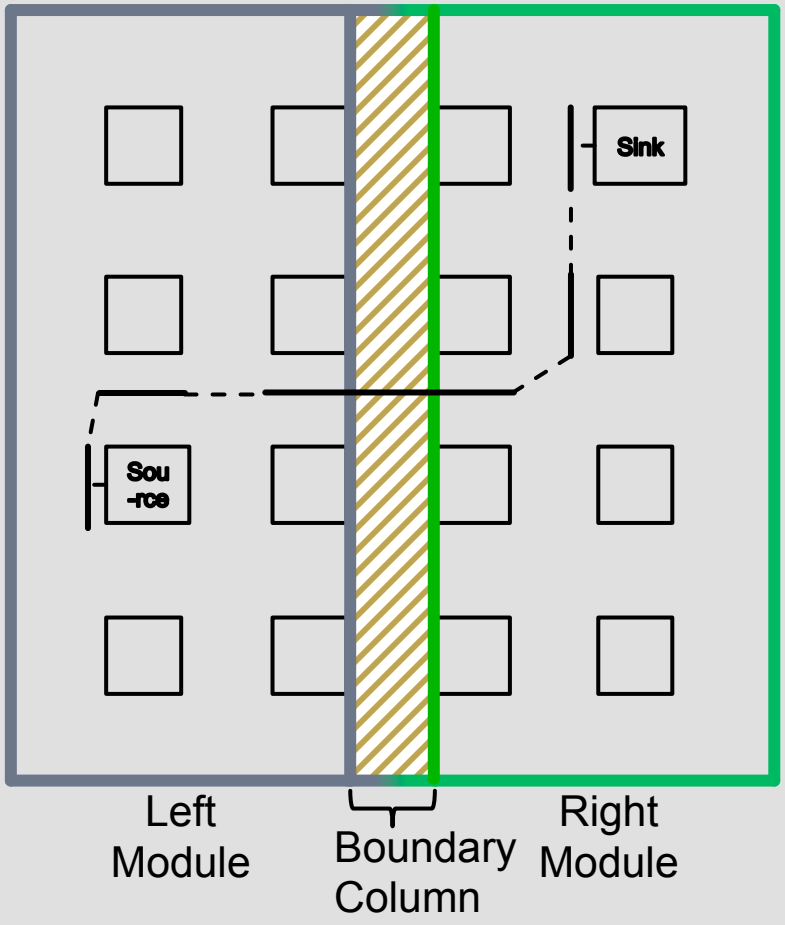
- Create 2 sides that we will then essentially route by abutment



Gives Rise to Two Types of Nets

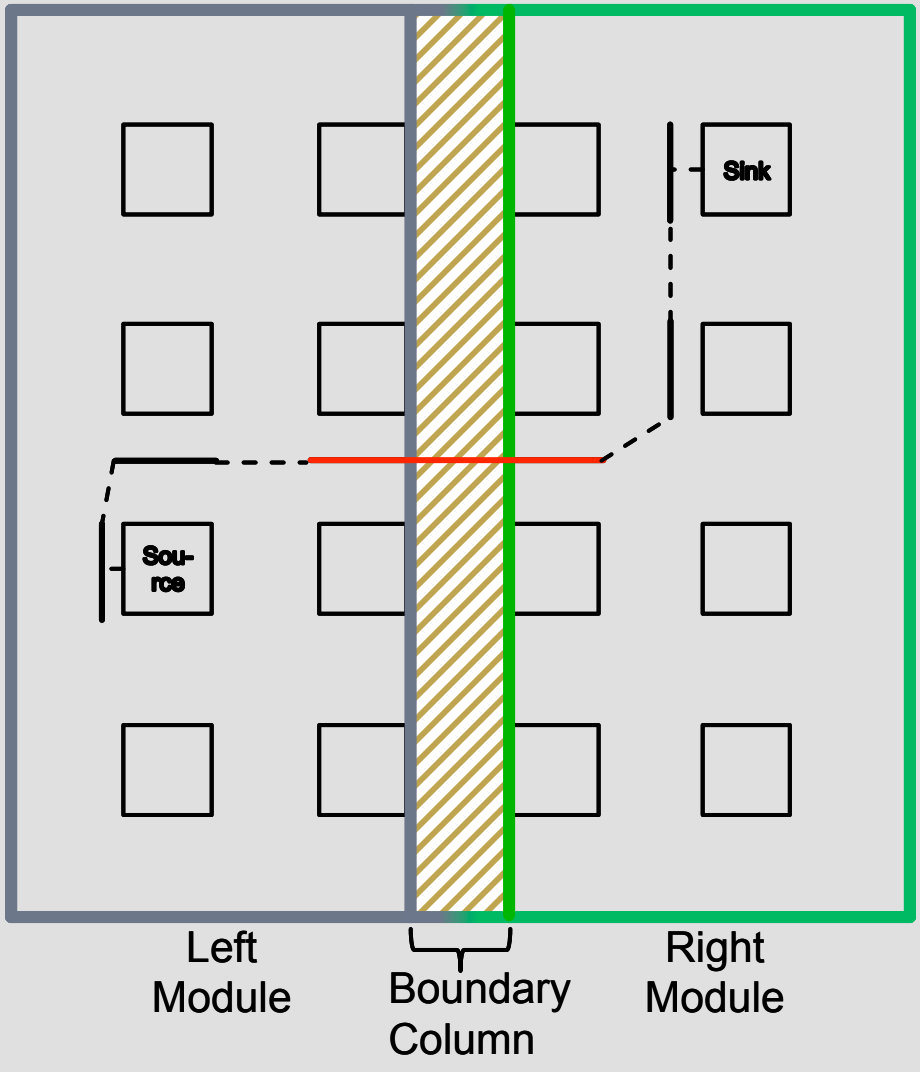


Single-Sided Nets

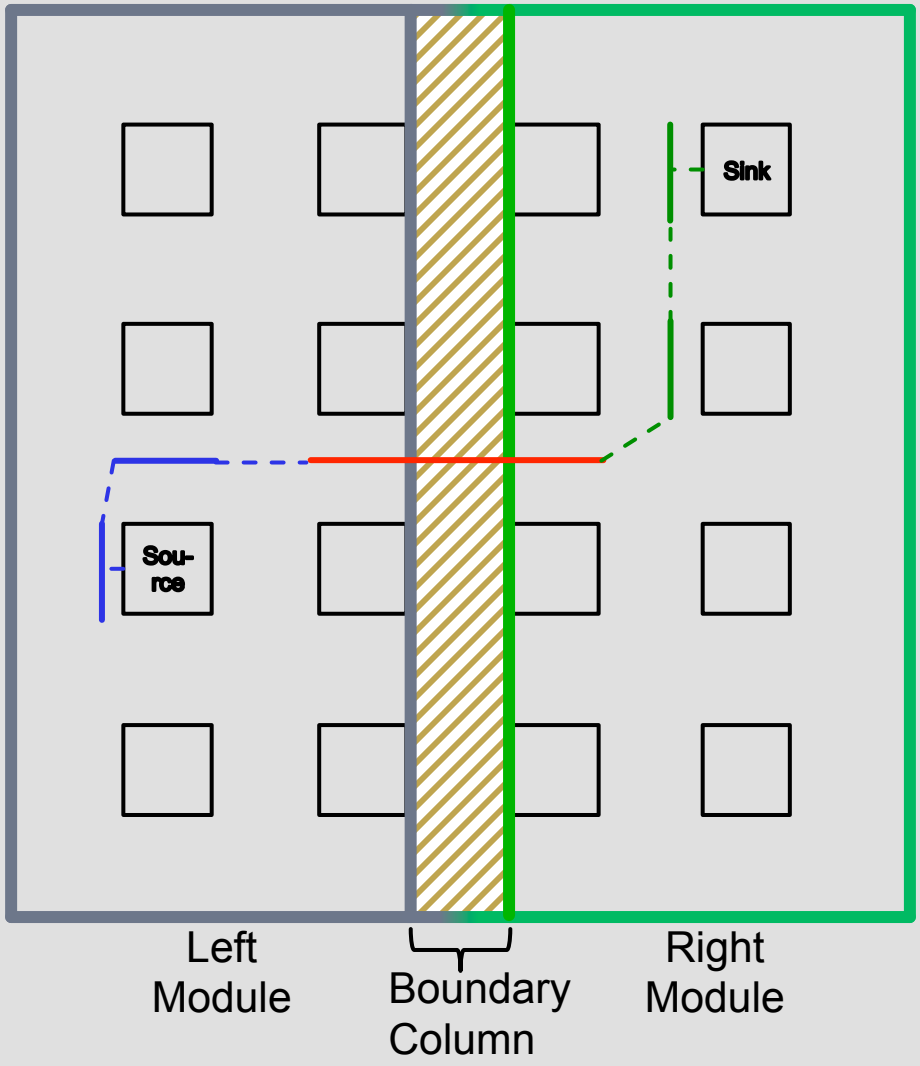


Double-Sided Nets

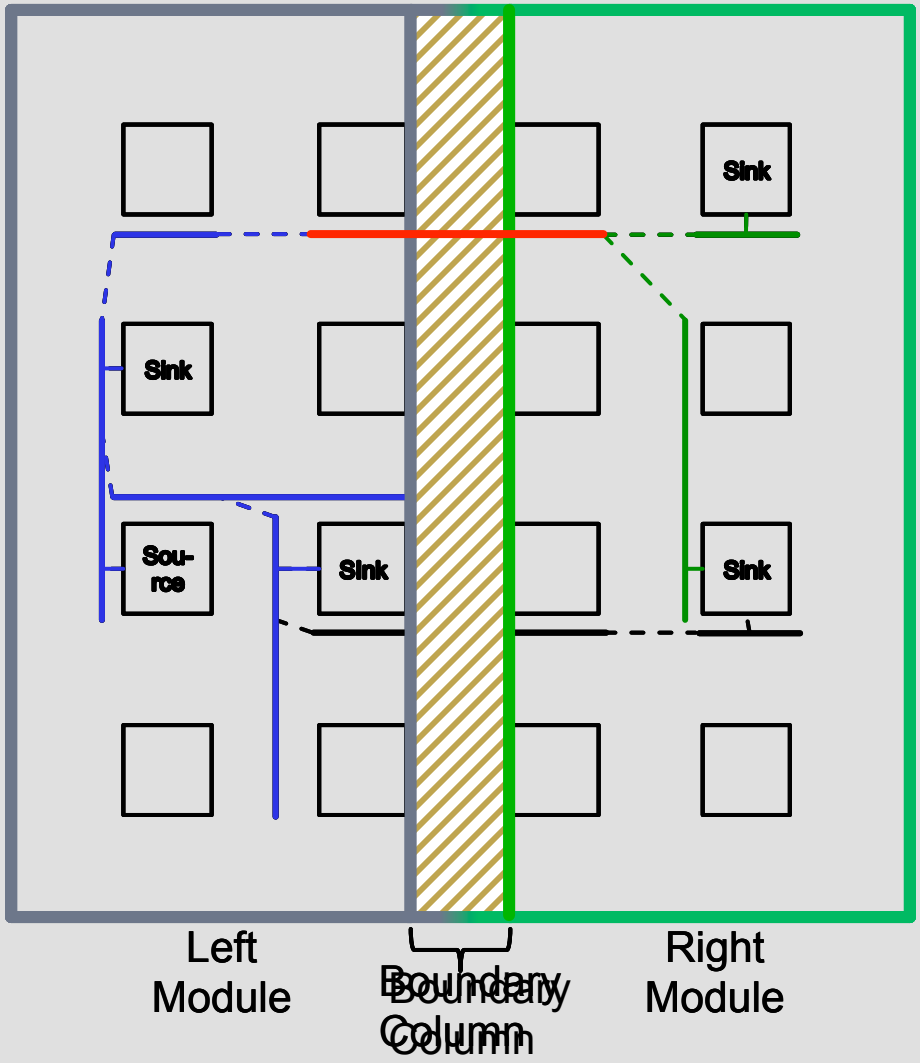
For 2-Sided Nets: Determine Target Segment



Turn Each 2-Sided Net into Two 'Faux' Nets



Issue: Double Sided Net With Multiple Crossings



Comparison

- **Base routing** – original circuit routed as usual
- **Split Routing** – route two sides independently

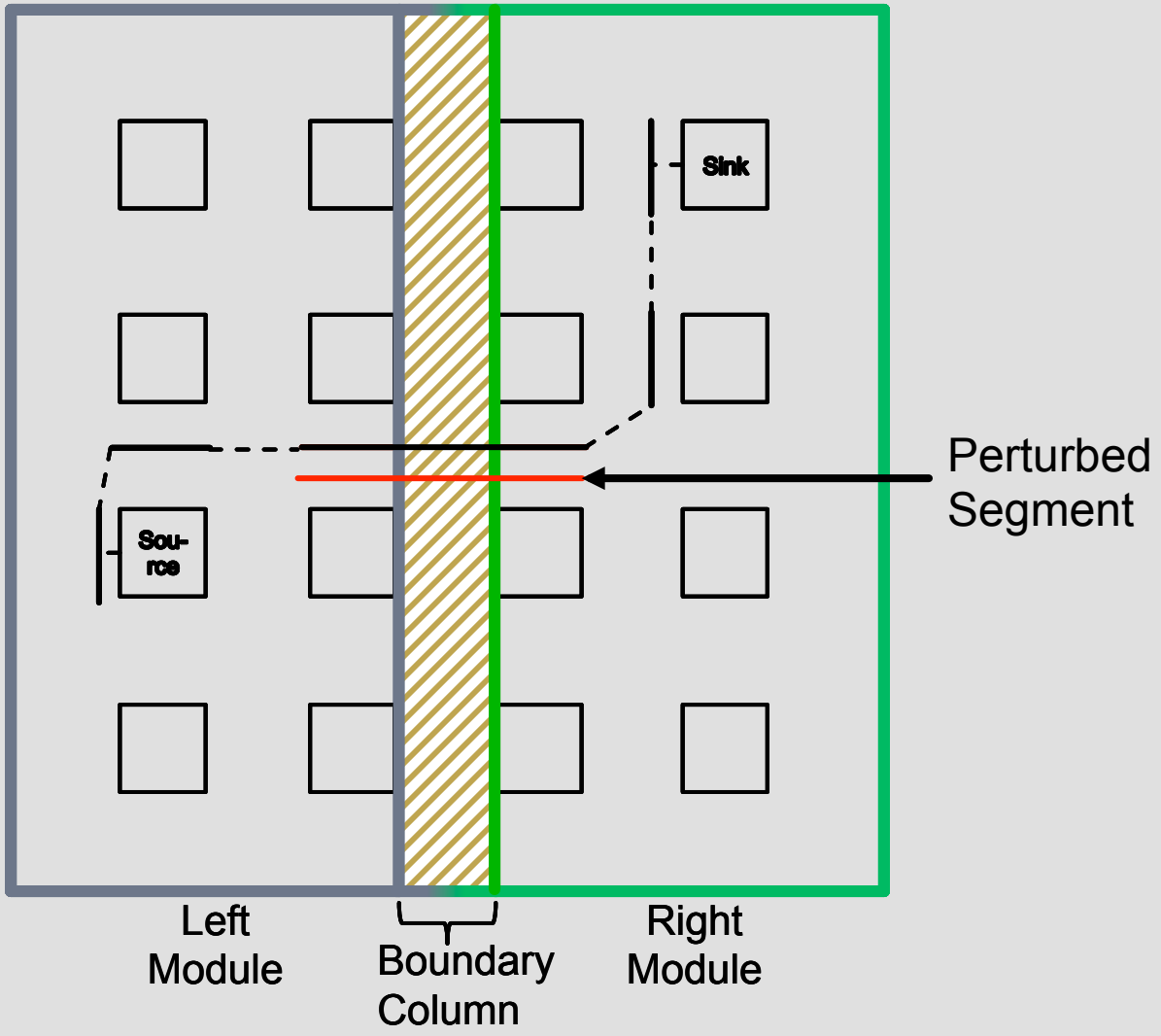
- What to expect?
- Shouldn't the answer be (almost) the same?
- Calculated the % increase of geometric mean of **Split** over **Base** for each metric

Base vs. Split Routing

Routed Wirelength	Critical Path Delay	Router Effort		Unroutes
		Heap Push #	Heap Pop #	
-4%	5%	11%	99%	2

- Decrease in wirelength can be attributed to:
  - On double-sided nets, multiple crossings are forbidden
    - total net length may end up shorter, but could increase critical path
  - borne out by increase in Critical Path Delay
- Results indicate that Pin-to-Wire Routing is quite inexpensive
  - However, target segment was chosen from Base Routing!
  - **Using this "Known Good Solution" is probably misleading**

More Realistic: ‘Split Perturbed’



Results: Split Perturb v. Base

Method (vs. Base)	Routed Wire length	Critical Path Delay	Router Effort		Un-routes
			Heap Push #	Heap Pop #	
Split	-4%	5%	11%	99%	2
Split Perturbed	6%	16%	66%	255%	2

- More difficulty apparent in significant increases
- Router is working much harder
- **However**, if target wire segments are not overly congested, pin-to-wire routing can succeed at some cost

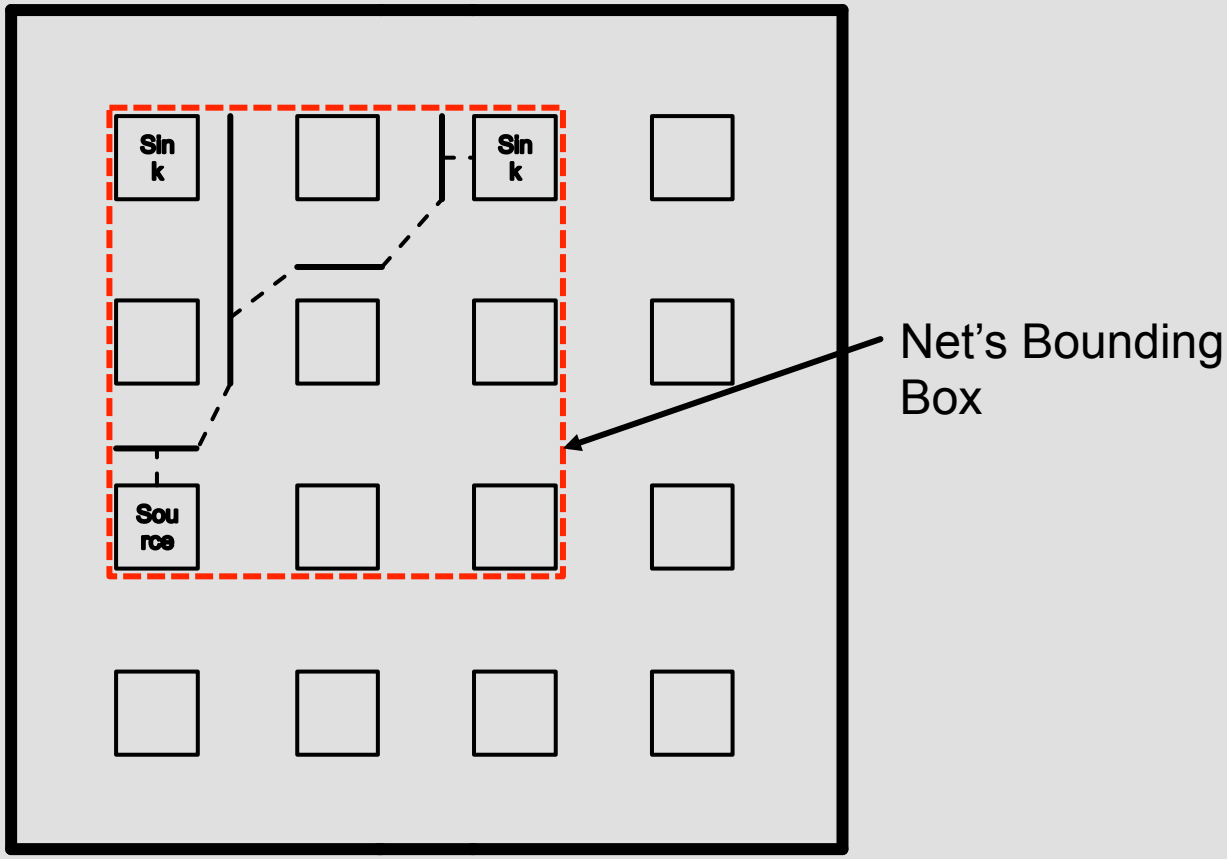
Dispersed Pin-to-Wire Routing

- Previous experiment has fixed amount of pin-to-wire routing
- Question: How much Pin-to-Wire Routing can be introduced in a circuit before significantly impacting its delay, area and router effort?
- Want to vary the amount of Pin-to-Wire Routing in a routing by varying the fraction, **F**, of nets being split

Methodology

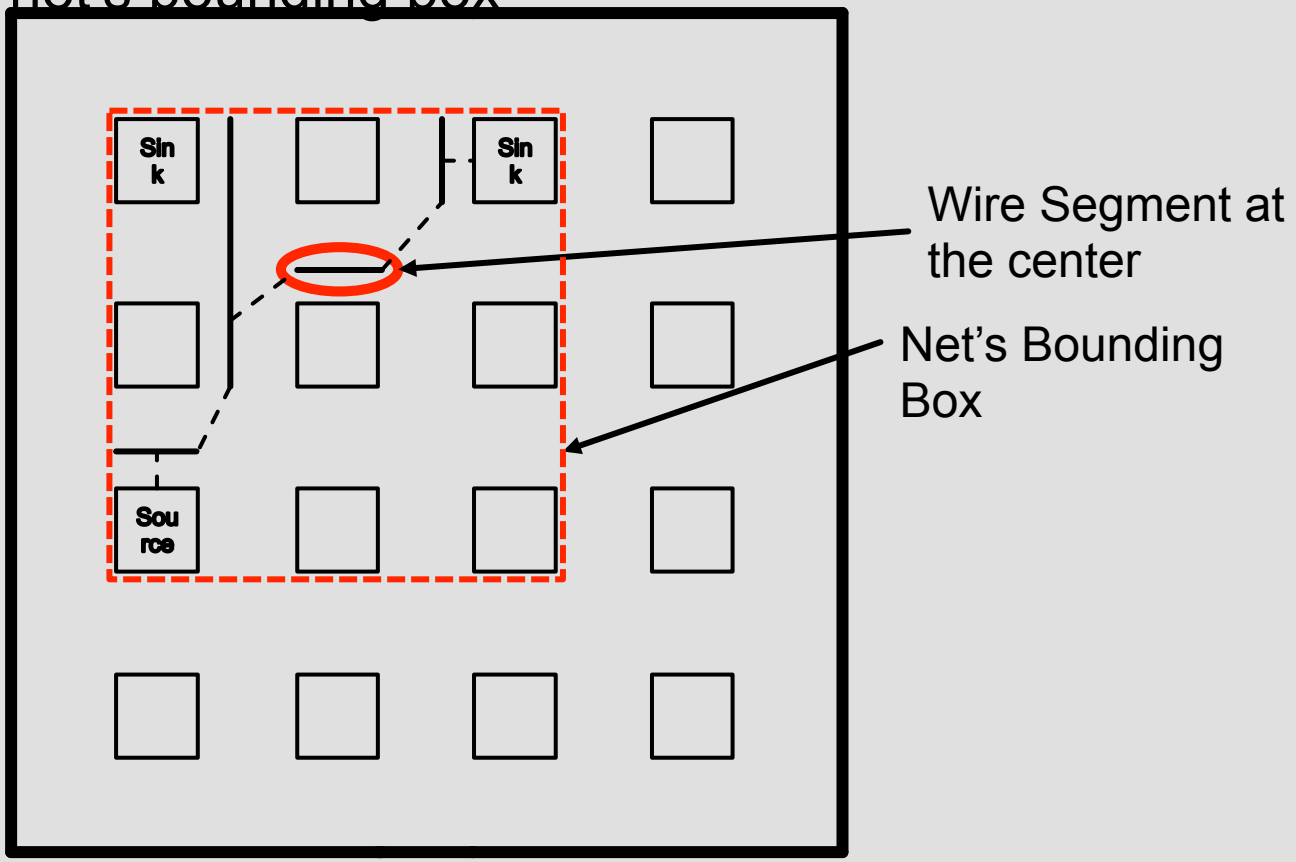
- **Base** measurement done as before
- **For each circuit** vary **F** from 0 to 100% of nets
  - Split each of those nets and do perturbed pin-to-wire routing on it

For each net to be split, determine net's bounding box

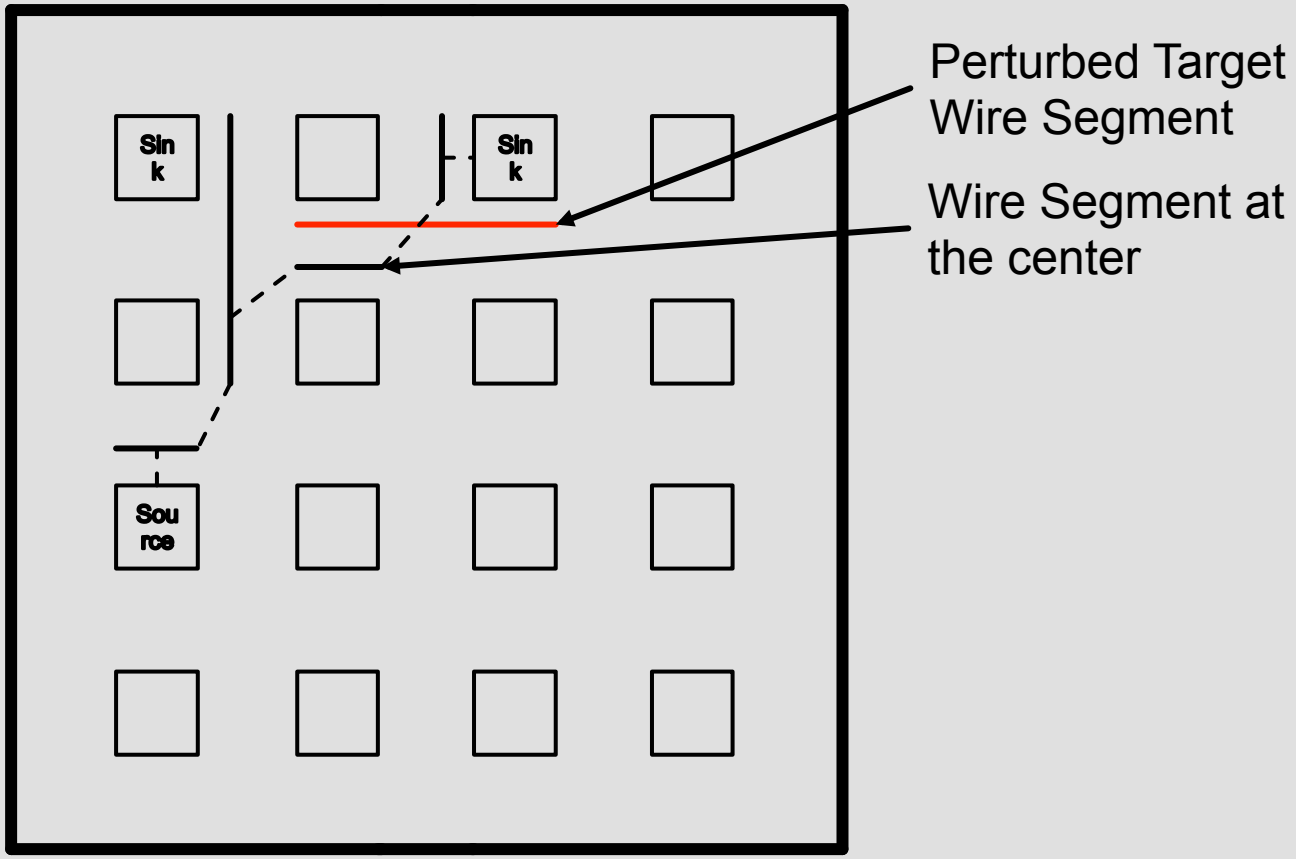


Next, pick a wire segment from the net's base routing

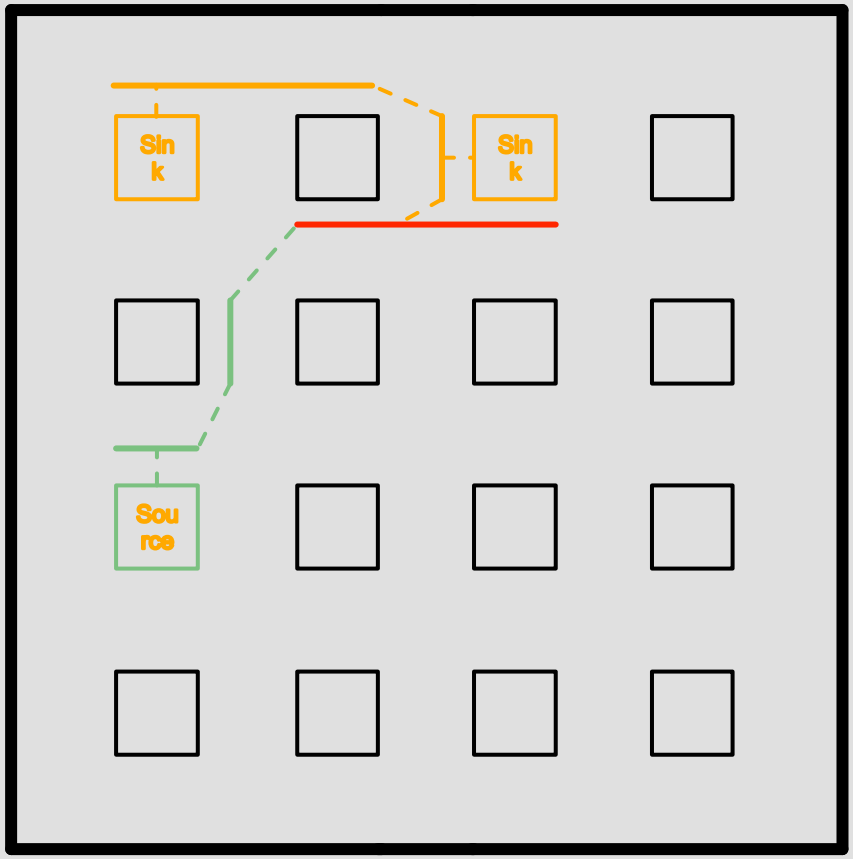
- Select a wire segment from the net's base routing, lying near the center of the net's bounding box



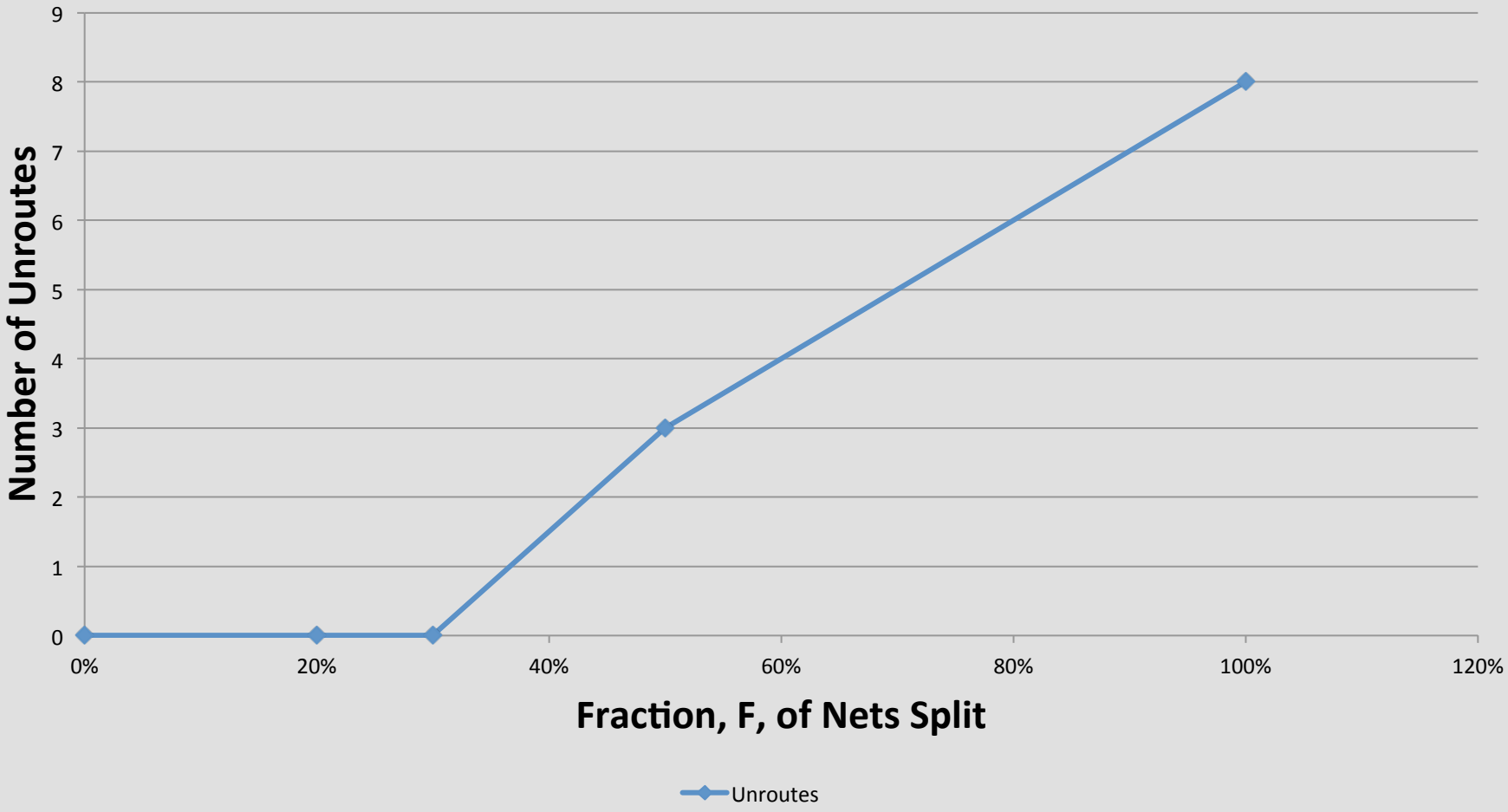
Acquire target wire segment by perturbing selected wire segment



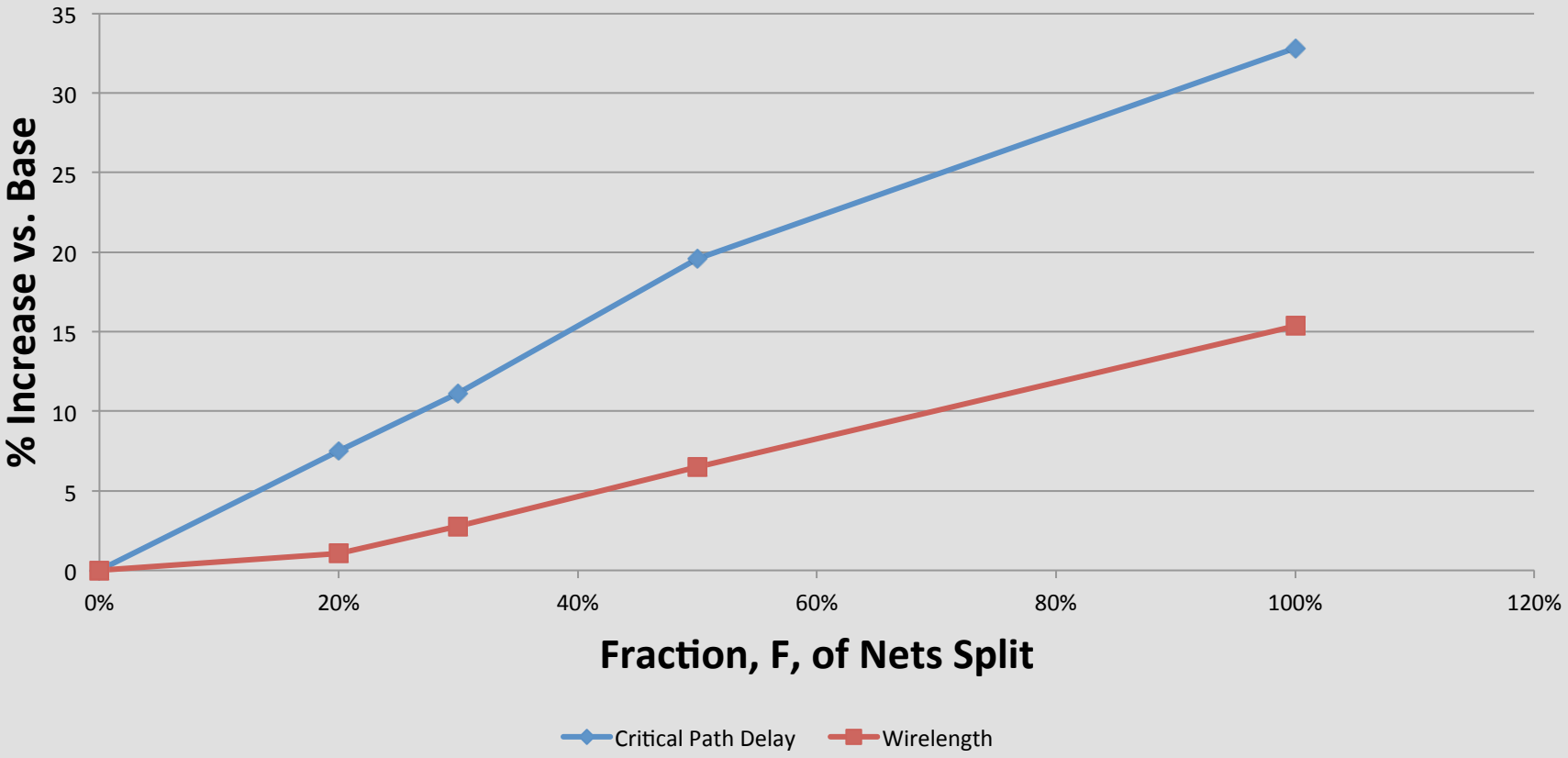
Create two faux nets



Unroutes vs. F

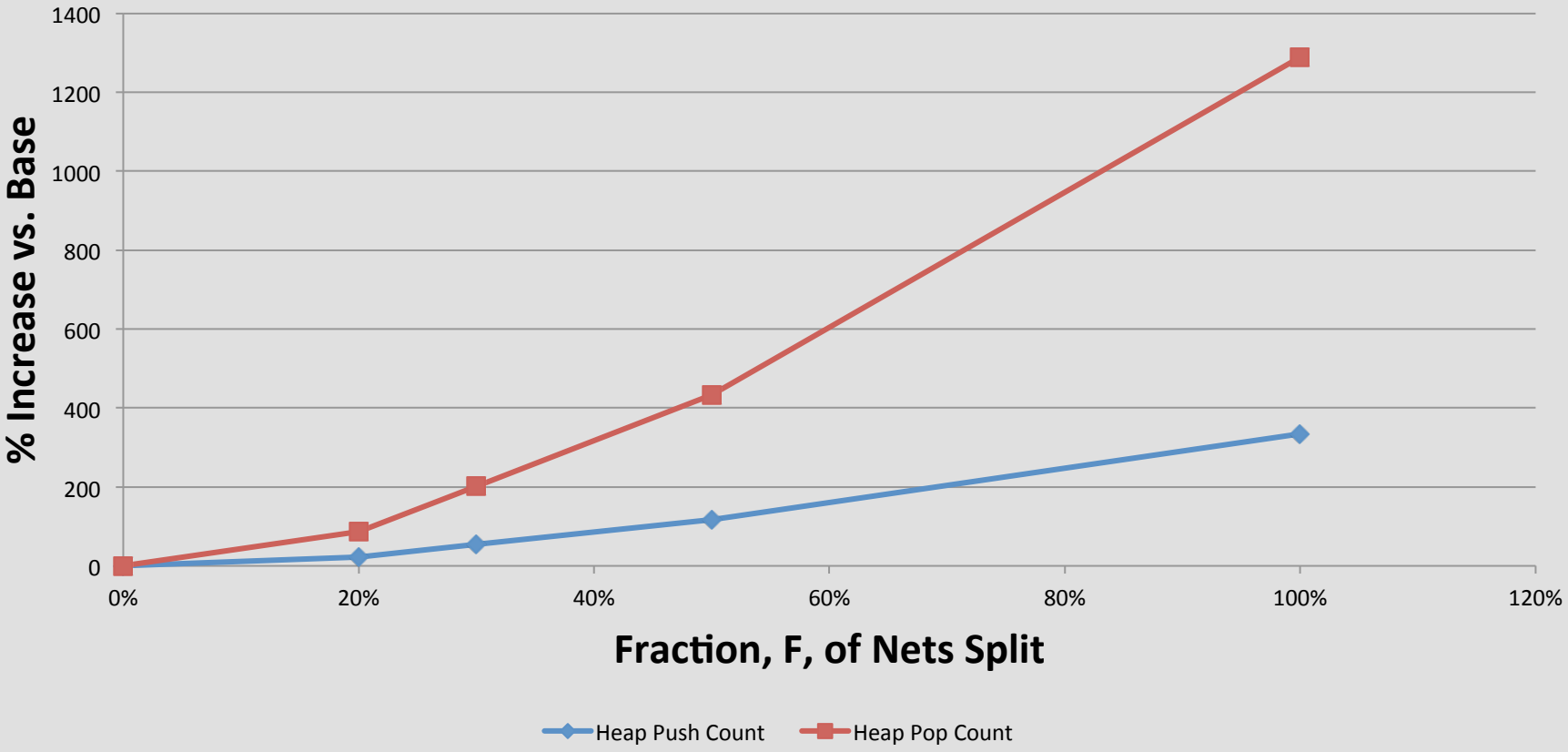


Wirelength & Delay vs. F



Variation in %increase over base for Wirelength and Critical Path Delay as a function of amount of pin-to-wire routing

Router Effort vs. F



Variation in %increase over base for Heap Push and Pop Count as a function of amount of pin-to-wire routing

Interpretation

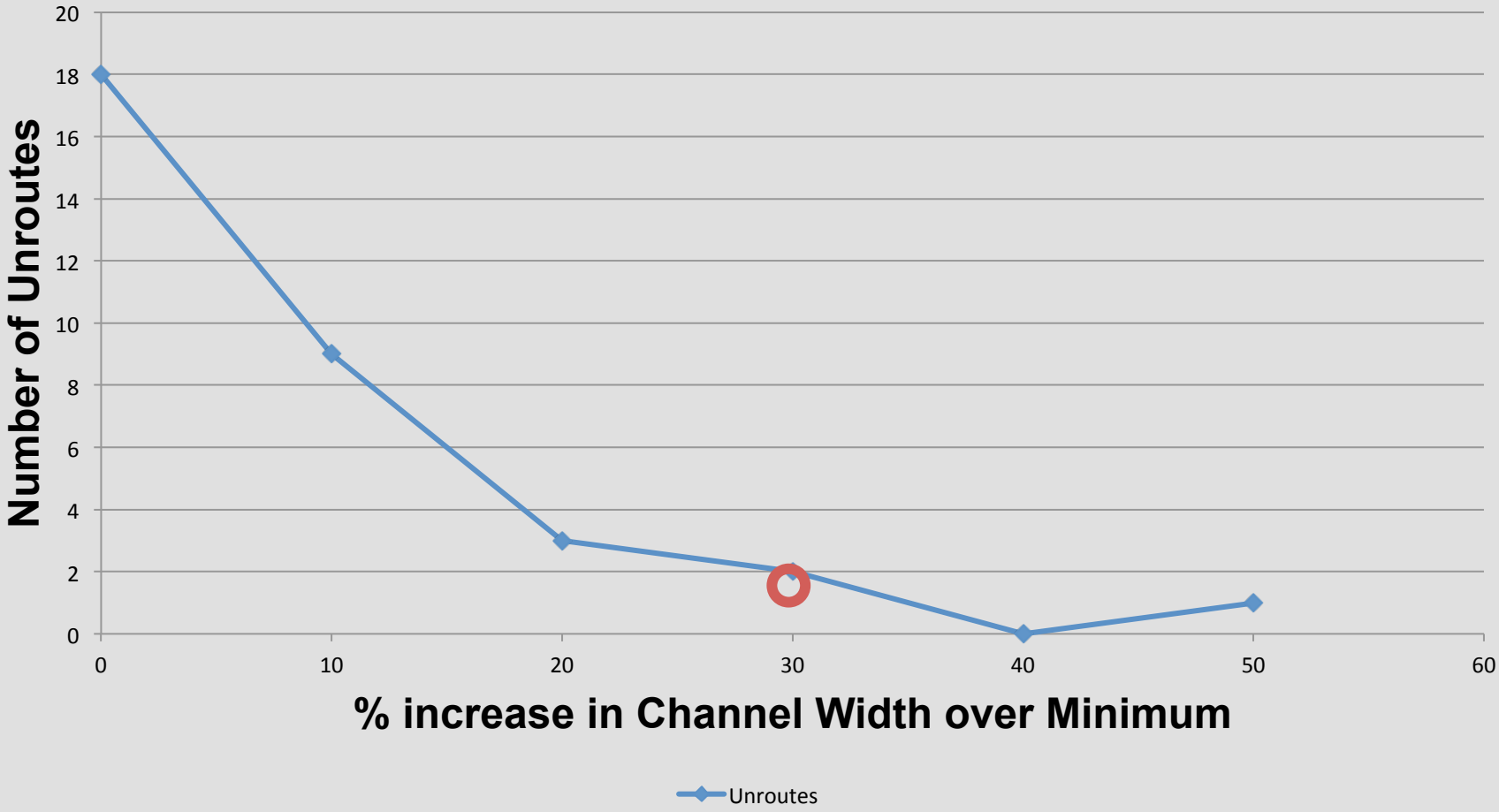
- Clearly, there is a price to be paid for increasing the amount of pin-to-wire routing
- The price is not always prohibitive

Effect of Track Count on Split Perturbed Pin-To-Wire Routing

- These results will vary depending on how hard the original routing problem is
  - Original experiments routed at min W + 30%
  - Will vary number of tracks/channel from 0% to +50%

- As track count increases, we expect:
  - the performance gap between pin-to-wire and pin-to-pin routing to reduce
  - unroutes to be eliminated

Unroutes vs. Extra Channel Width



Conclusions and Current Work

- Measured the difficulty faced by a router and a routing architecture in the face of pin-to-wire routing
- Significant increase in wirelength, critical path delay, and router effort and some loss of routability
  - But tolerable under some circumstances
- Future Work: Measure impact of routing architecture (Fs, Fc, etc.) on Pin-to-Wire Routing

Questions?