Bio-Inspired Walking: A FPGA multicore system for a legged robot

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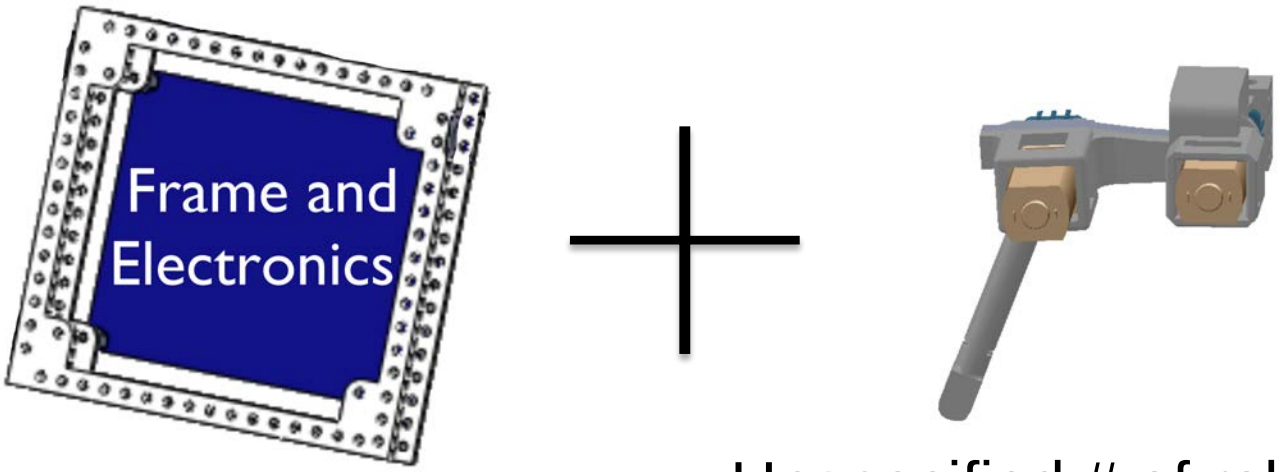
Motivation

Design: Legged robot platform for research

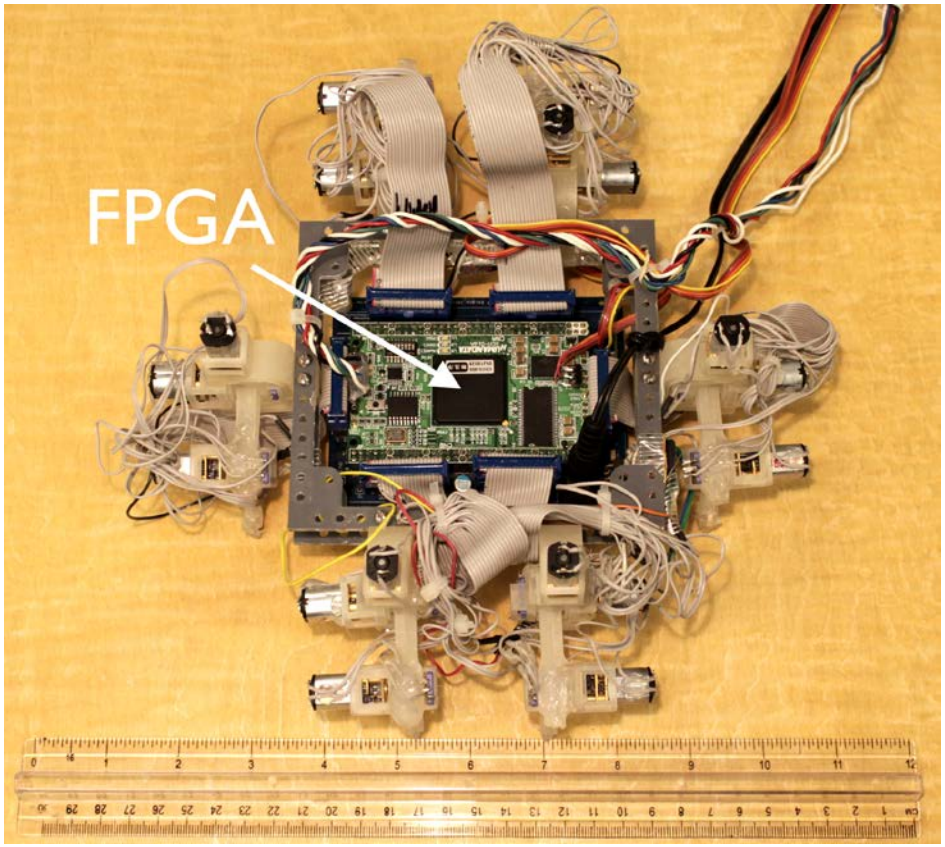


Unspecified # of robot legs

Needed: **Flexible**, **Easy**, and **Low Latency** control architecture

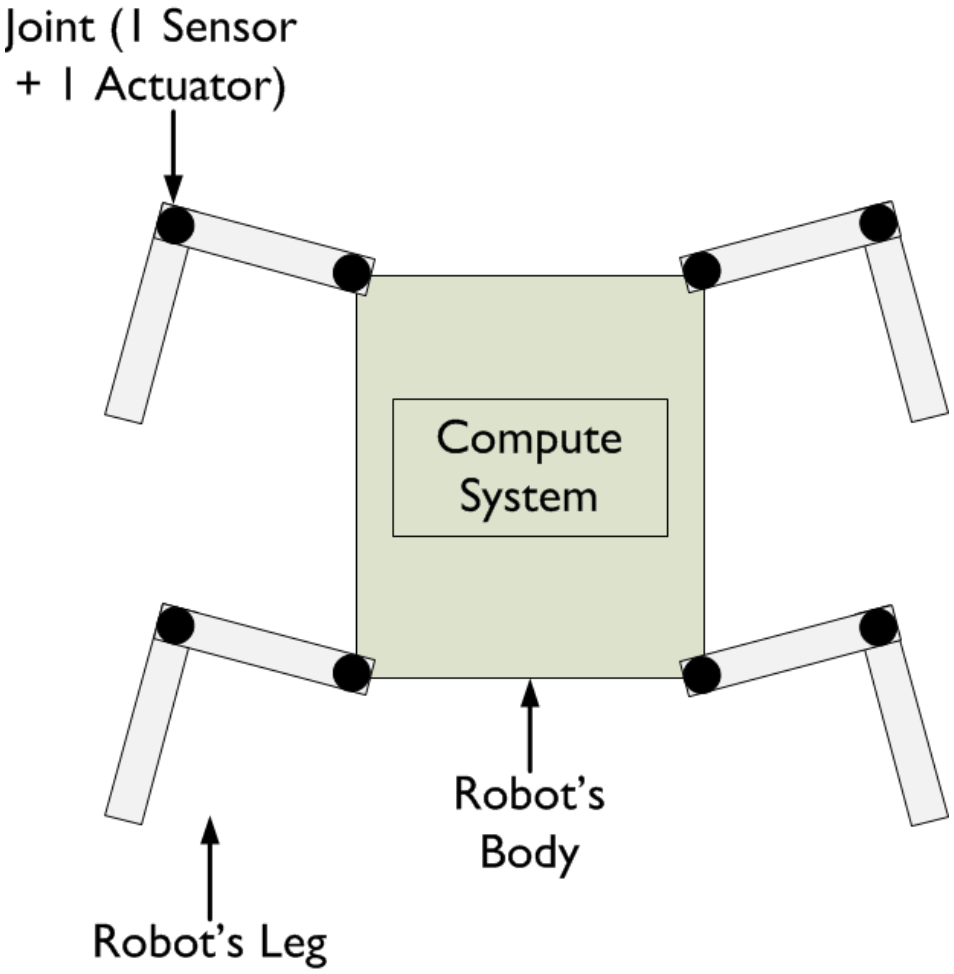
Outline

- Previous solutions
- Proposed solution
  - Architecture
  - Results
- Conclusion
  - Future work
  - Questions



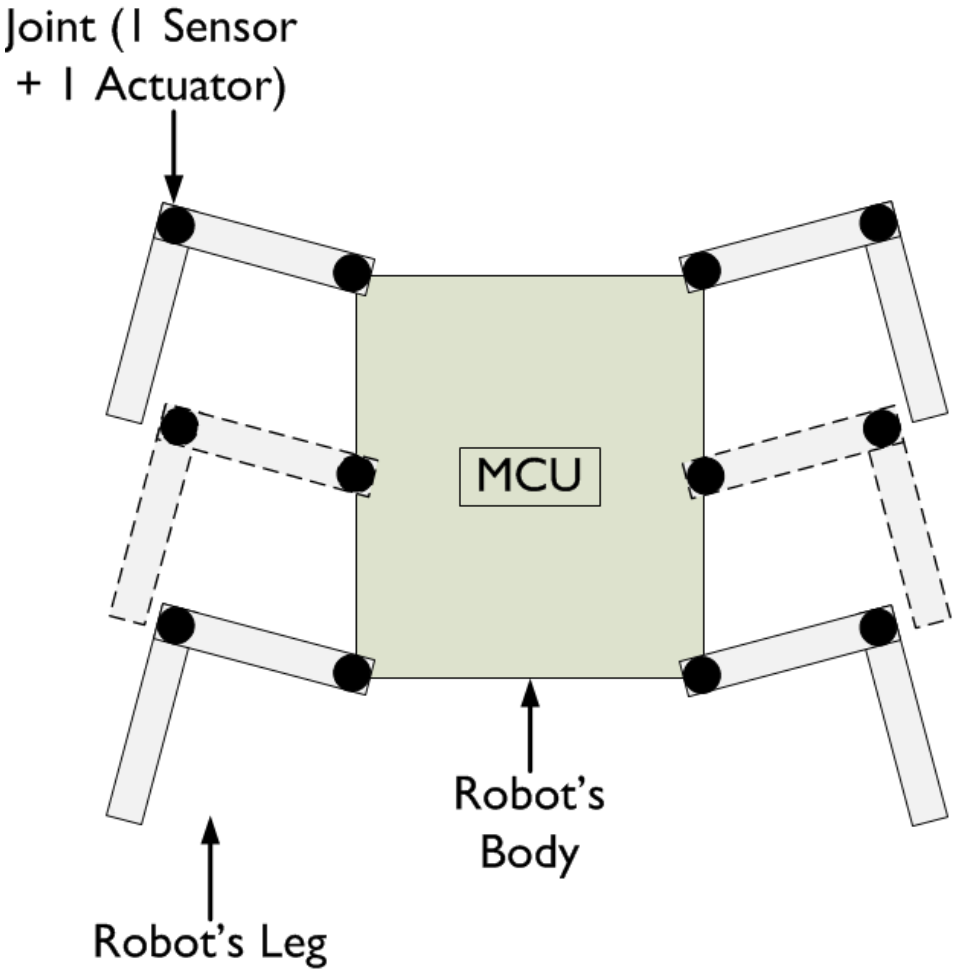
A top view of Abigaille-III on a lab desk

System Requirements



- High specialty pin count:
  - Analog/Digital Converters (ADCs)
  - Pulse Width Modulation (PWM)

Previous Solution #1

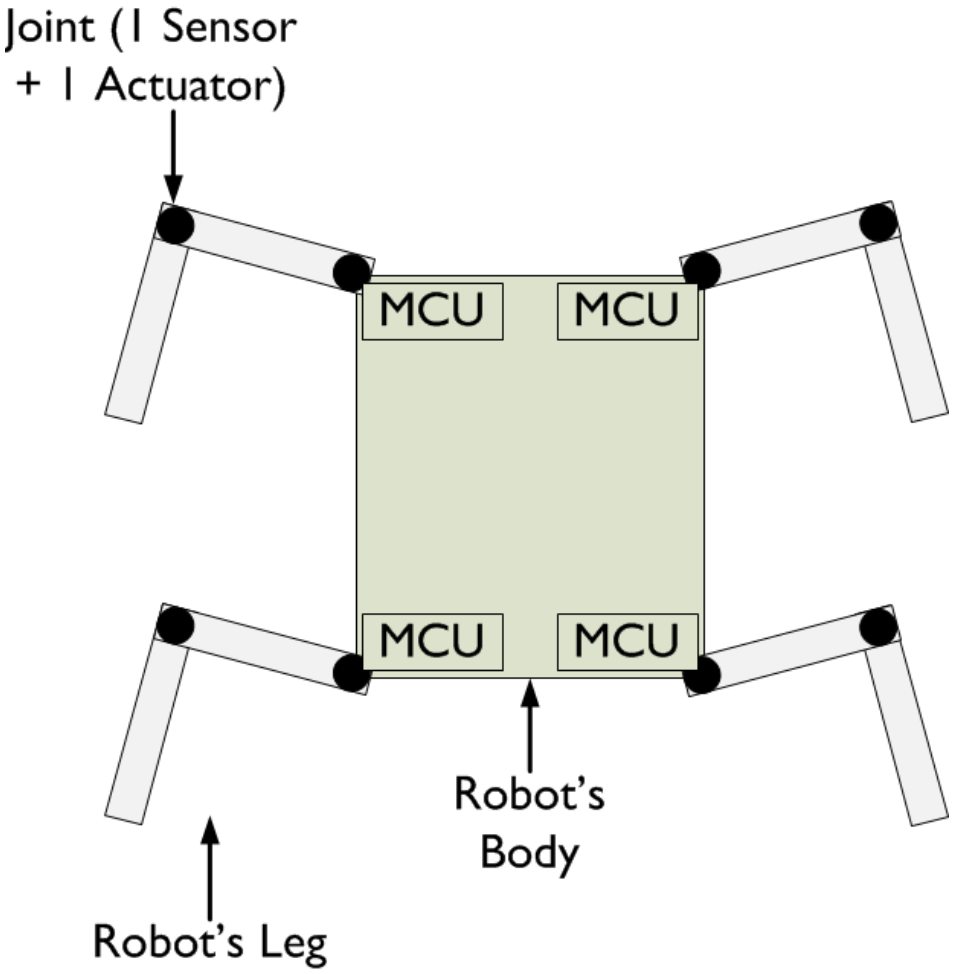


Con:

- Changing loop frequency

Single processor, single control loop [1-2]

Previous Solution #2

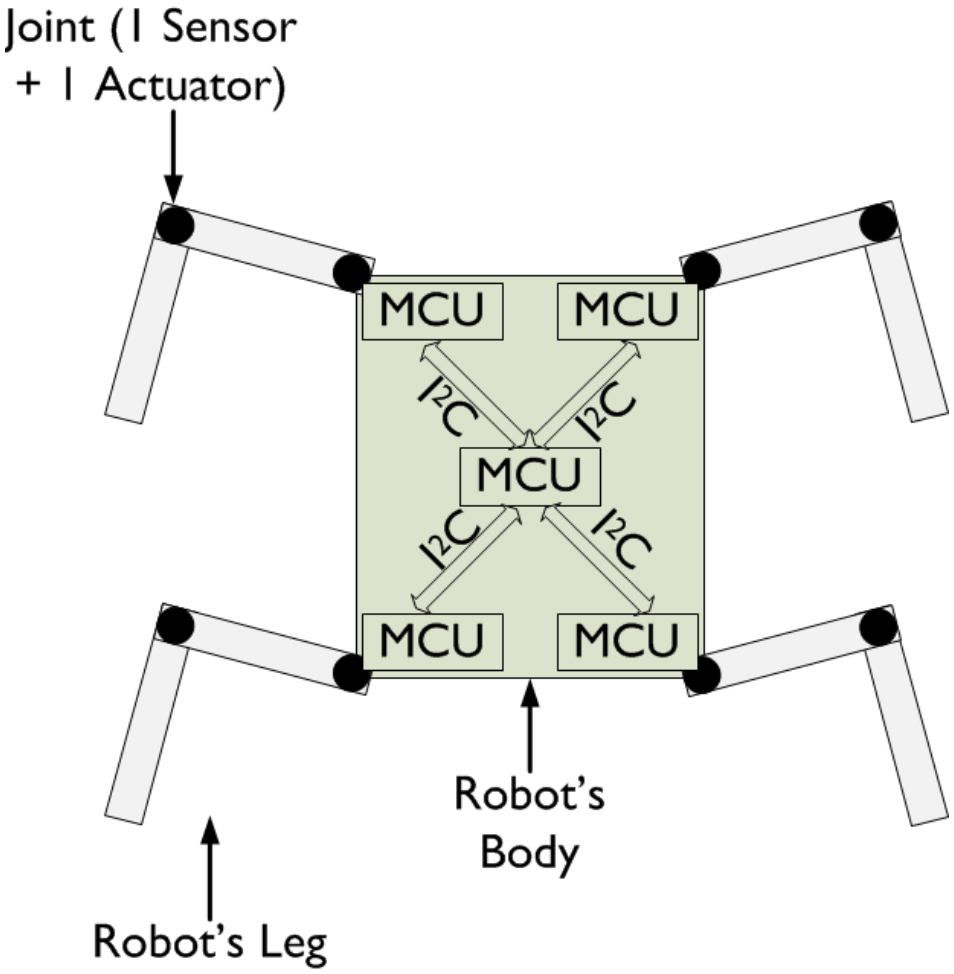


Cons:

- Physical size
- Power consumption

Multiple processors, multiple control loops [3-5]

Previous Solution #2

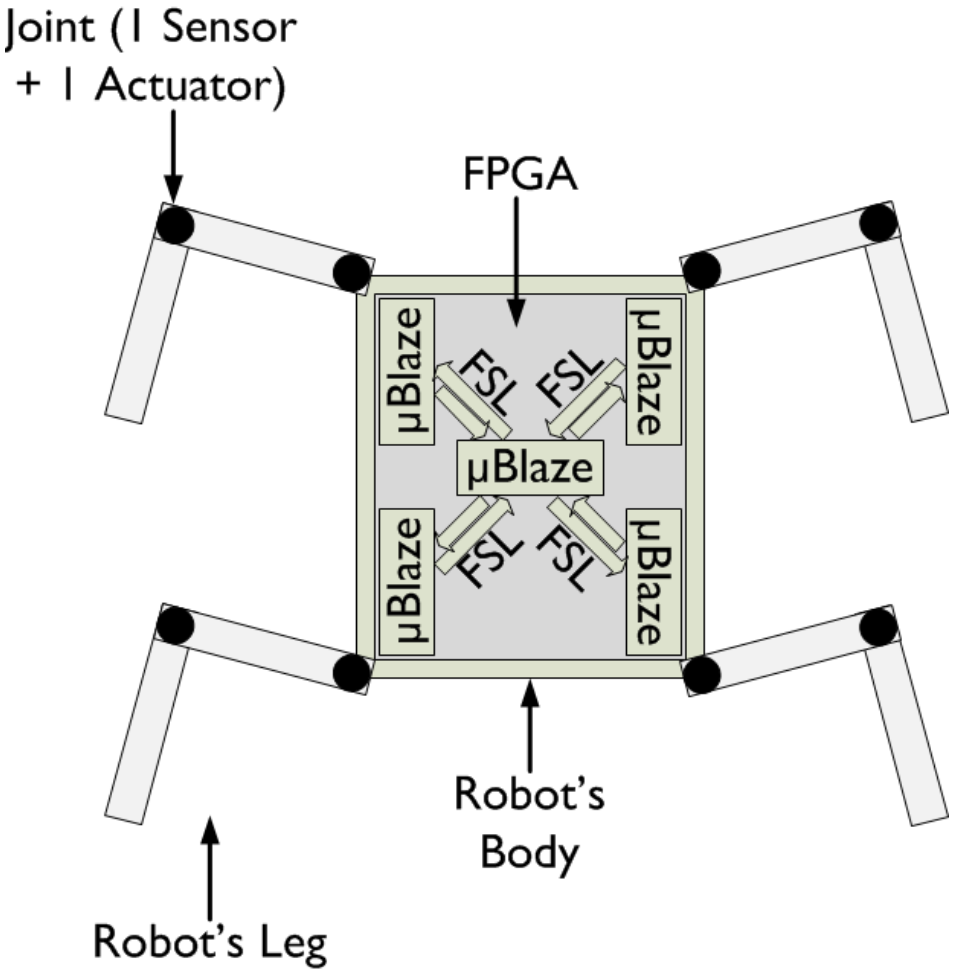


Con:

- Interprocessor communication latency

Multiple processors, multiple control loops [3-5]

Proposed Solution



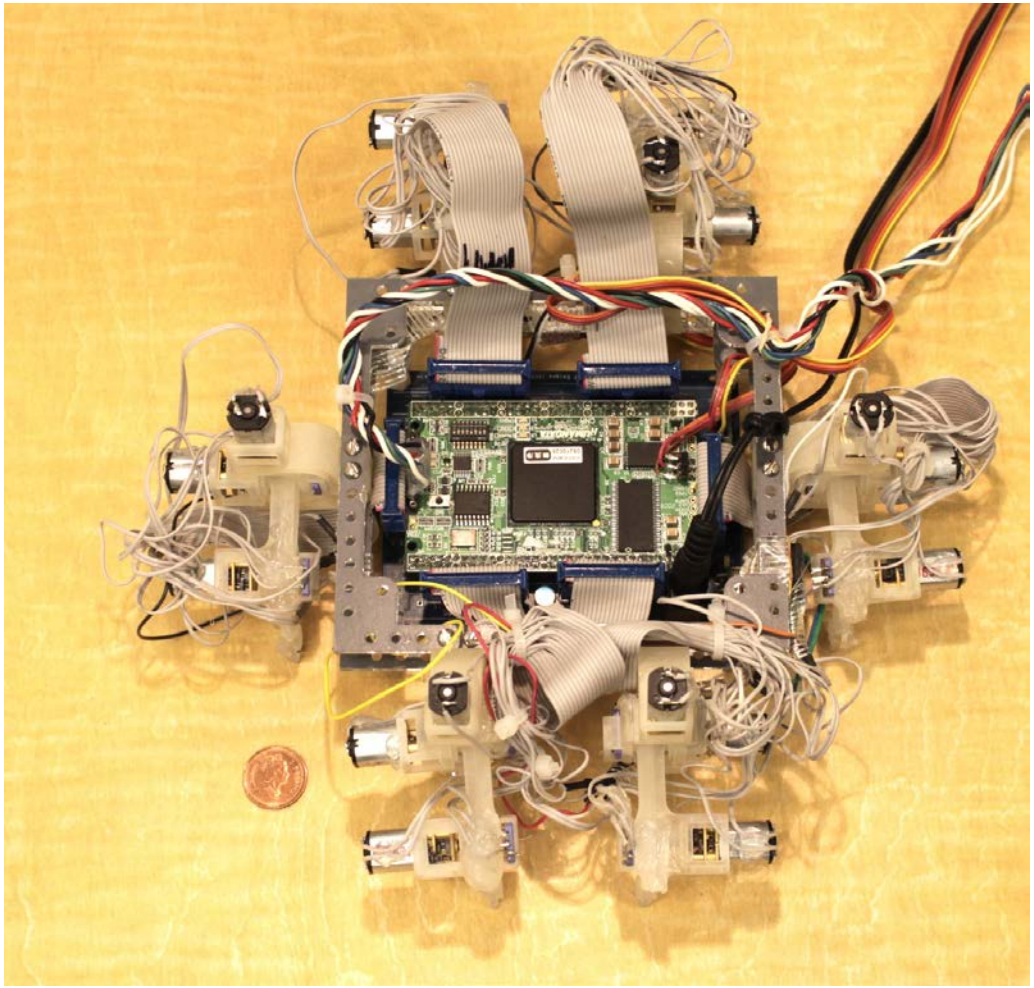
Pro:

- Reconfigure to match mechanical system!

Proposed System Advantages

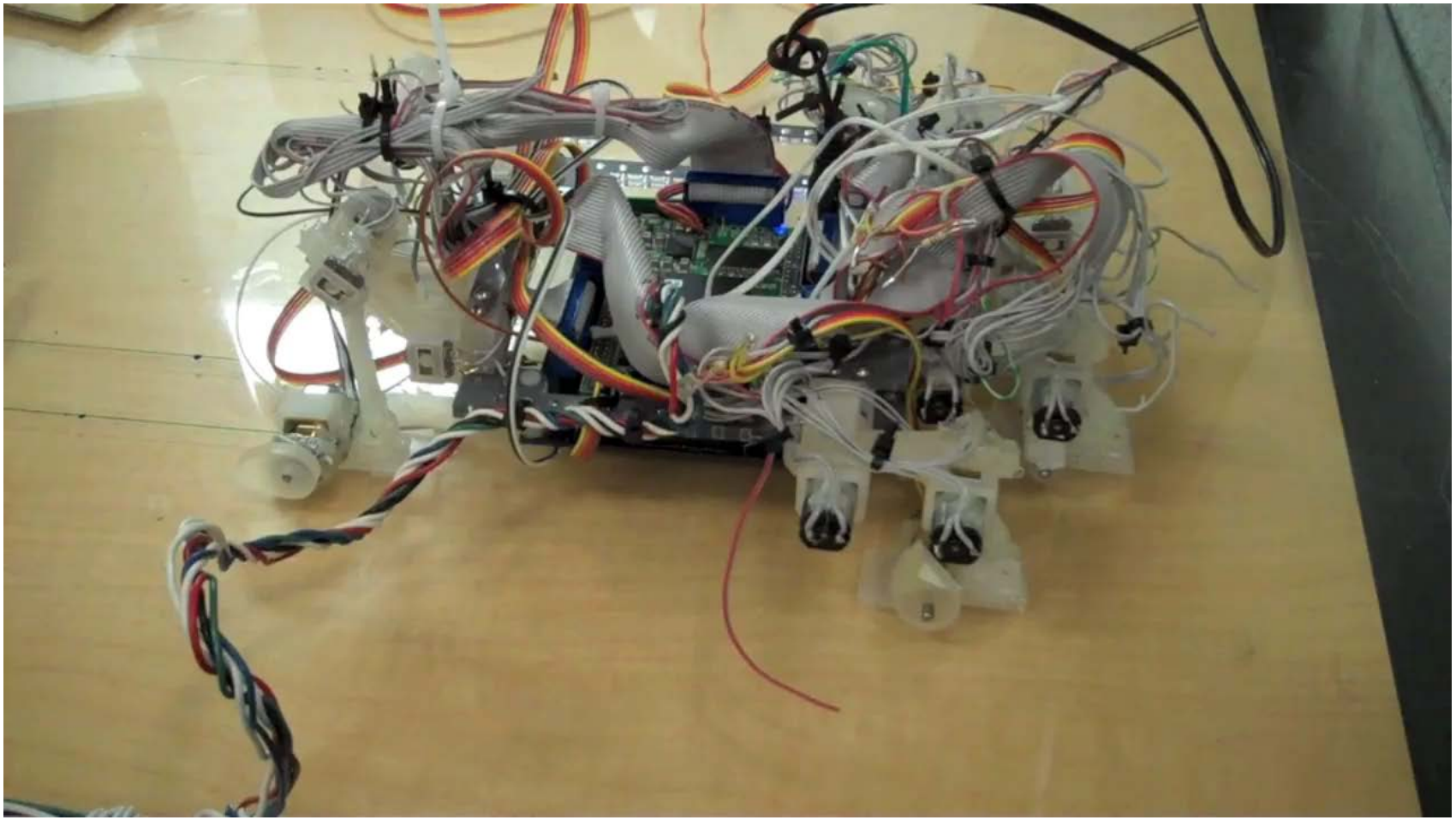
- Loop frequency constant
- PWMs and ADCs can be generated in hardware
- Low interprocessor communication latency

Our Robot



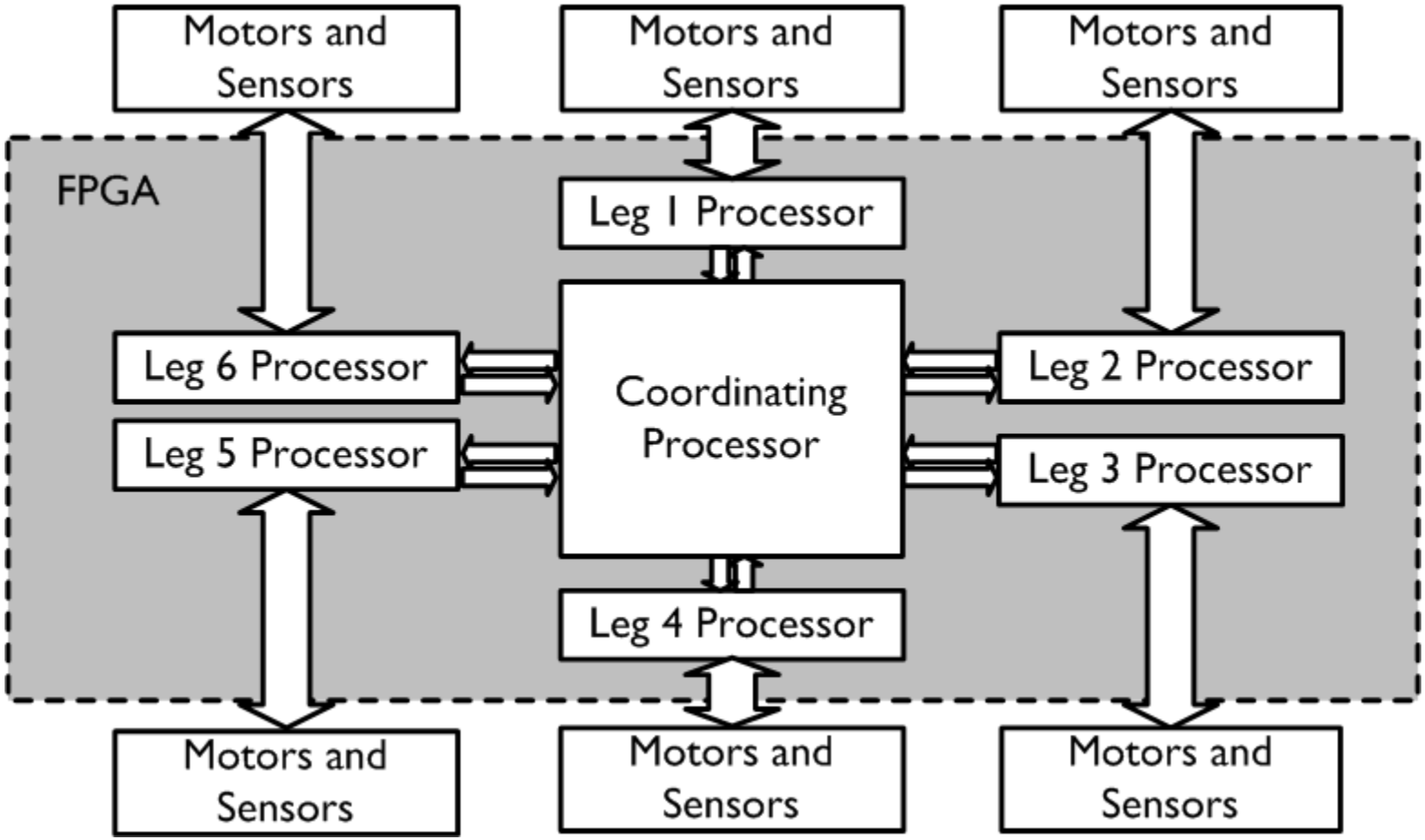
Approximate Dimensions: 20 cm x 20 cm x 20 cm

Our Robot

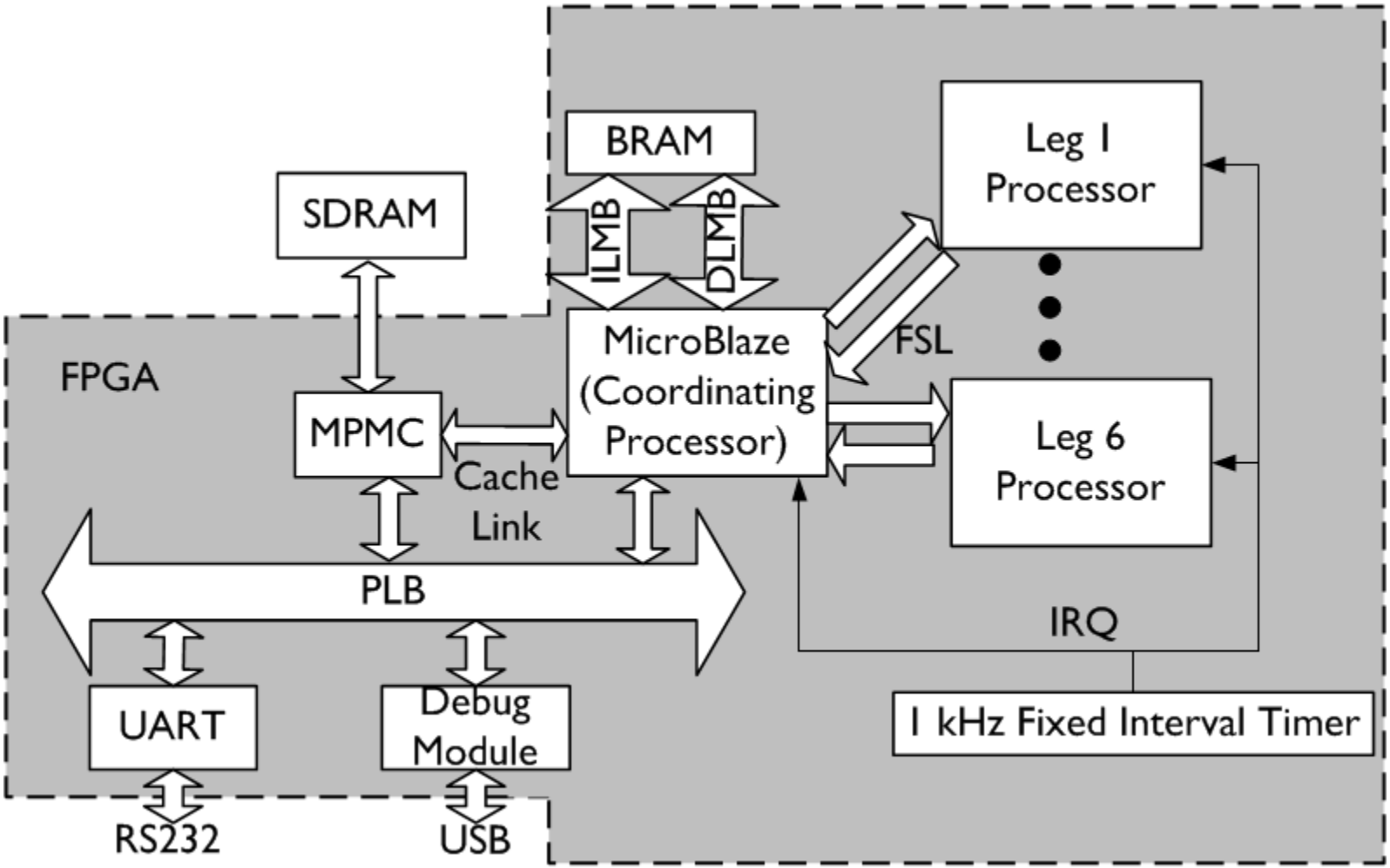


Average body speed: 1 mm·s^{-1}

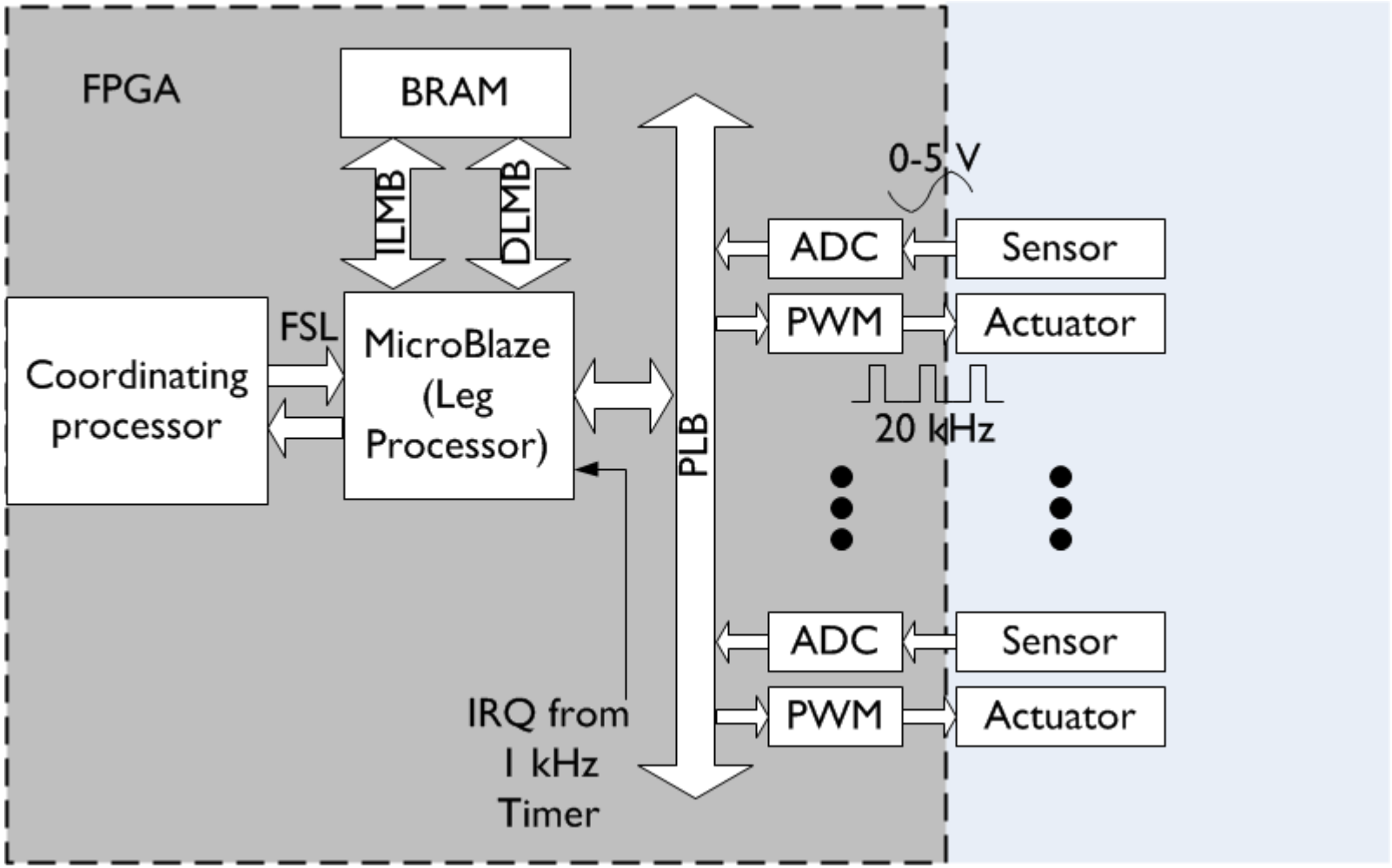
System Overview



Coordinating Processor

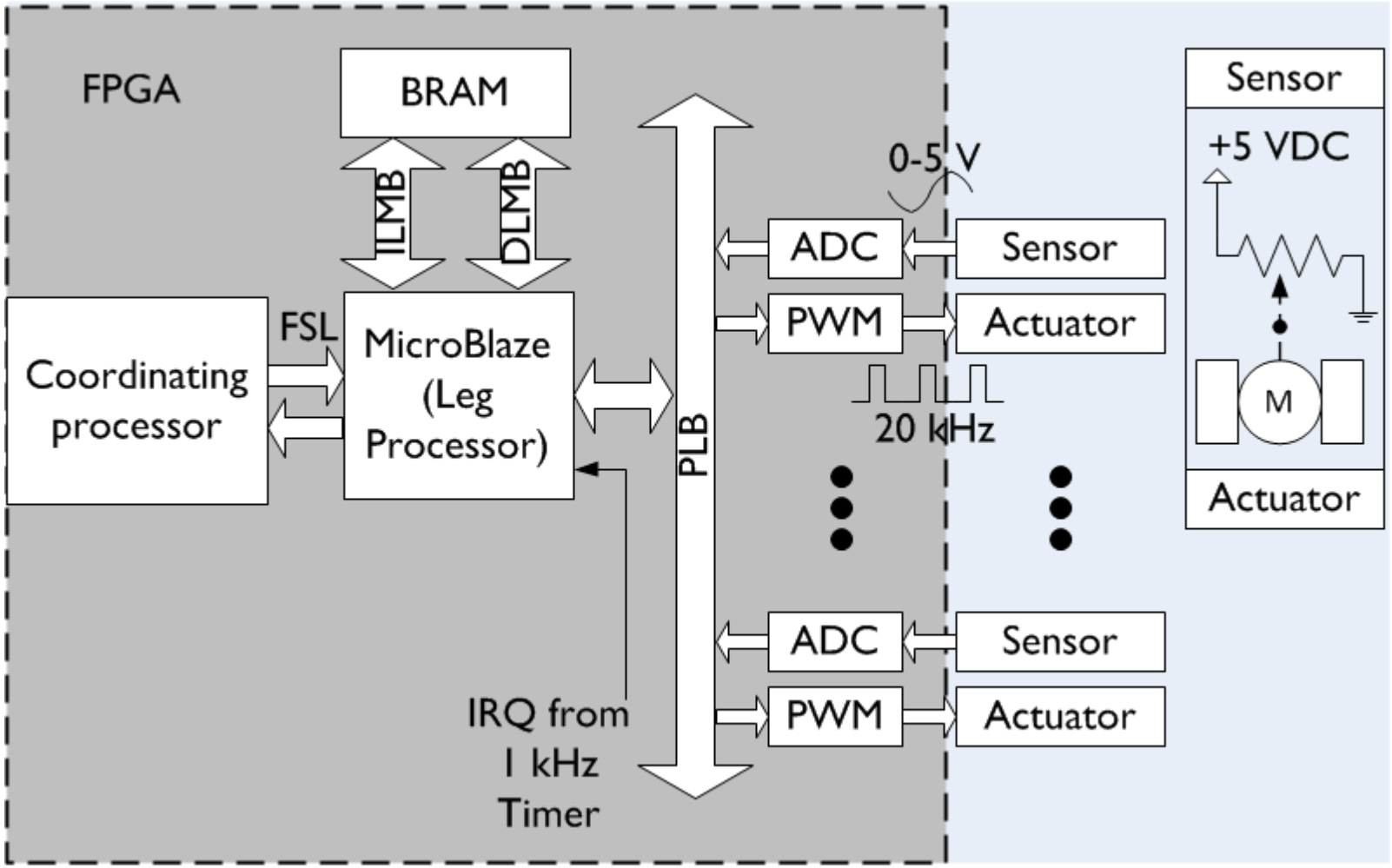


Robot Leg Processor



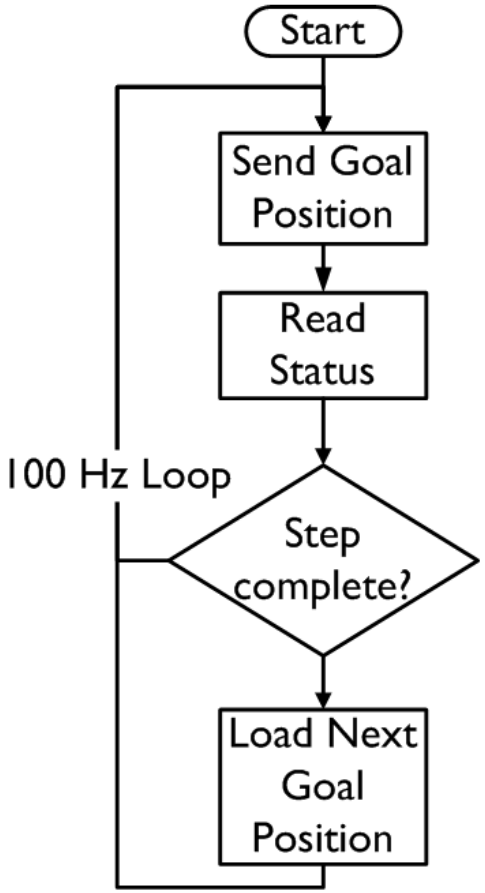
Structure is repeated for each robot leg

Robot Leg Processor

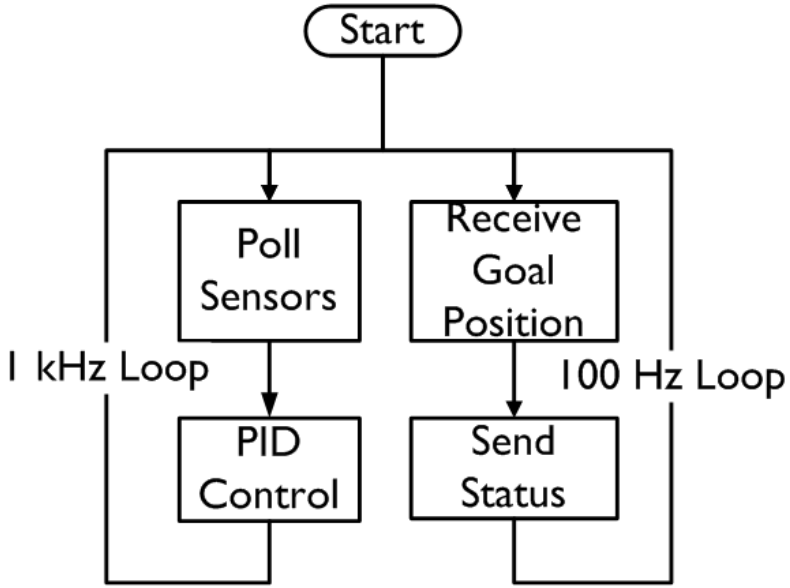


Structure is repeated for each robot leg

System Software



Coordinating Processor



Leg Control Processors

System Requirements

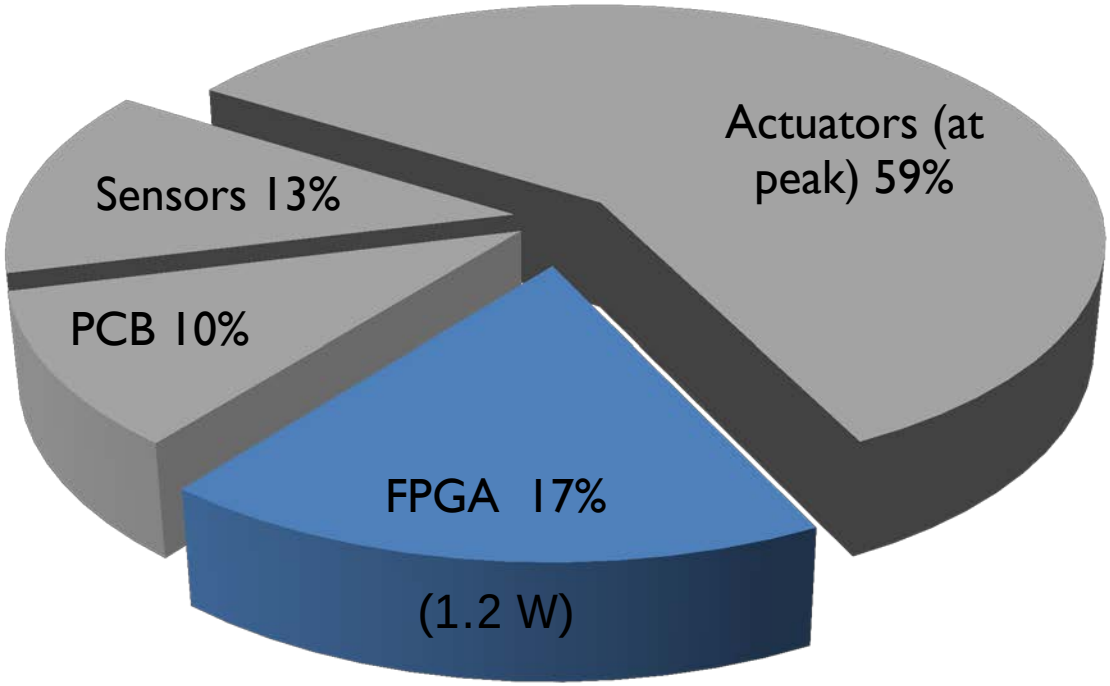
FPGA Resource	Usage	Usage (%)
Flip Flops	27362	57
LUTs	33491	70
User I/Os	90	90
DSPs	23	18
BRAMs	112	89
Processor Code Space	**Usage (B)**	**Usage (%)**
Leg Processors	23928	73
Coordinating Processor	21500	<1

FPGA is a Spartan 3A DSP FGG676

Implementation Frequencies

Subsystem		Frequency
Low level control loop	Software capability	12 kHz
	ADC capability	2 kHz
	Implementation	1 kHz
Interprocessor updates		100 Hz
System clock		50 MHz

System Power Consumption



Total: 6.8 W

Future Work

- Reduce power consumption
  - Slow down system clock (estimated 0.8 W vs. current 1.2 W)
- More complex low level controller
- Higher levels of control
- Heterogeneous FPGA with ARM processor

Summary

Objective	Solution
Flexibility	Reconfigurable electronics (FPGA)
Ease of use	Modular architecture
Low latency	FSL (Processors on same silicon)

Questions?

Thanks for your attention!

References

Single processor, single control loop robots:

[1] H. Bingshan, L. Wang, Y. Zhao, and Z. Fu, “A miniature wall climbing robot with biomechanical suction cups,” *Industrial Robot: An International Journal*, vol. 36, no. 6, pp. 551-561, 2009.

[2] M. P. Murphy and M. Sitti, “Waalbot: An agile small-scale wall-climbing robot utilizing dry elastomer adhesives,” *IEEE/ASME Transactions on Mechatronics*, vol. 12, no. 3, pp. 330-338, Jun. 2007.

Multiple processor, multiple control loop robots:

[3] S. Kim, M. Spenko, S. Trujillo, B. Heyneman, V. Mattoli, and M. R. Cutkosky, “Whole body adhesion: hierarchical, directional and distributed control of adhesive forces for a climbing robot,” in *Robotics and Automation, 2007 IEEE International Conference on*, pp. 1268-1273, 2007.

[4] M. J. Spenko, G. C. Haynes, J. A. Saunders, M. R. Cutkosky, A. A. Rizzi, R. J. Full, and D. E. Koditschek, “Biologically inspired climbing with a hexapedal robot,” *Journal of Field Robotics*, vol. 25, no. 4-5, pp. 223-242, Apr. 2008.

[5] Y. Li, A. Ahmed, D. Sameoto, and C. Menon, “Abigaille II: toward the development of a spider-inspired climbing robot,” *Robotica*, vol. 30, pp. 79-89, Apr. 2012

Added Path Planner