Bio-Inspired Walking: A FPGA multicore system for a legged robot

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Motivation

*Design:* Legged robot platform for research

*Needed:* Flexible, Easy, and Low Latency control architecture

Unspecified # of robot legs
Outline

• Previous solutions
• Proposed solution
  – Architecture
  – Results
• Conclusion
  – Future work
  – Questions
System Requirements

- High specialty pin count:
  - Analog/Digital Converters (ADCs)
  - Pulse Width Modulation (PWM)
Previous Solution #1

Con:
- Changing loop frequency

Single processor, single control loop [1-2]
Previous Solution #2

Cons:
- Physical size
- Power consumption

Multiple processors, multiple control loops [3-5]
Previous Solution #2

Con:
- Interprocessor communication latency

Multiple processors, multiple control loops [3-5]
Proposed Solution

Pro:
- Reconfigure to match mechanical system!
Proposed System
Advantages

• Loop frequency constant

• PWMs and ADCs can be generated in hardware

• Low interprocessor communication latency
Our Robot

Approximate Dimensions: 20 cm x 20 cm x 20 cm
Our Robot

Average body speed: 1 mm·s$^{-1}$
System Overview
Coordinating Processor
Robot Leg Processor

Structure is repeated for each robot leg
Robot Leg Processor

Structure is repeated for each robot leg
System Software

Coordinating Processor

100 Hz Loop

Start

Send Goal Position

Read Status

Step complete?

Load Next Goal Position

1 kHz Loop

Poll Sensors

PID Control

Send Status

1 kHz Loop

Receive Goal Position

Leg Control Processors

100 Hz Loop
System Requirements

<table>
<thead>
<tr>
<th>FPGA Resource</th>
<th>Usage</th>
<th>Usage (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flip Flops</td>
<td>27362</td>
<td>57</td>
</tr>
<tr>
<td>LUTs</td>
<td>33491</td>
<td>70</td>
</tr>
<tr>
<td>User I/Os</td>
<td>90</td>
<td>90</td>
</tr>
<tr>
<td>DSPs</td>
<td>23</td>
<td>18</td>
</tr>
<tr>
<td>BRAMs</td>
<td>112</td>
<td>89</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Processor Code Space</th>
<th>Usage (B)</th>
<th>Usage (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leg Processors</td>
<td>23928</td>
<td>73</td>
</tr>
<tr>
<td>Coordinating Processor</td>
<td>21500</td>
<td>&lt;1</td>
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</tbody>
</table>

FPGA is a Spartan 3A DSP FGG676
# Implementation Frequencies

<table>
<thead>
<tr>
<th>Subsystem</th>
<th>Frequency</th>
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<tbody>
<tr>
<td>Low level control loop</td>
<td></td>
</tr>
<tr>
<td>Software capability</td>
<td>12 kHz</td>
</tr>
<tr>
<td>ADC capability</td>
<td>2 kHz</td>
</tr>
<tr>
<td>Implementation</td>
<td>1 kHz</td>
</tr>
<tr>
<td>Interprocessor updates</td>
<td>100 Hz</td>
</tr>
<tr>
<td>System clock</td>
<td>50 MHz</td>
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</tbody>
</table>
System Power Consumption

- Actuators (at peak) 59%
- Sensors 13%
- PCB 10%
- FPGA 17%

(1.2 W)

Total: 6.8 W
Future Work

• Reduce power consumption
  – Slow down system clock (estimated 0.8 W vs. current 1.2 W)

• More complex low level controller

• Higher levels of control

• Heterogeneous FPGA with ARM processor
## Summary

<table>
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<th>Objective</th>
<th>Solution</th>
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<tbody>
<tr>
<td>Flexibility</td>
<td>Reconfigurable electronics (FPGA)</td>
</tr>
<tr>
<td>Ease of use</td>
<td>Modular architecture</td>
</tr>
<tr>
<td>Low latency</td>
<td>FSL (Processors on same silicon)</td>
</tr>
</tbody>
</table>
Questions?

Thanks for your attention!
References

Single processor, single control loop robots:


Multiple processor, multiple control loop robots:


Added Path Planner