Profiling FPGA Floor-planning Effects on Timing Closure

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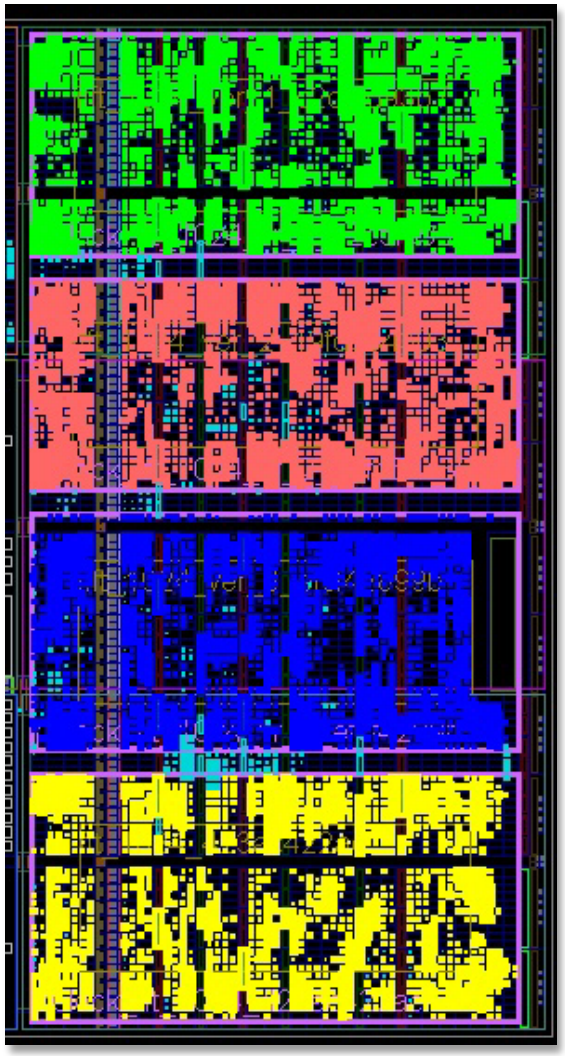
FPGA Floor-planning

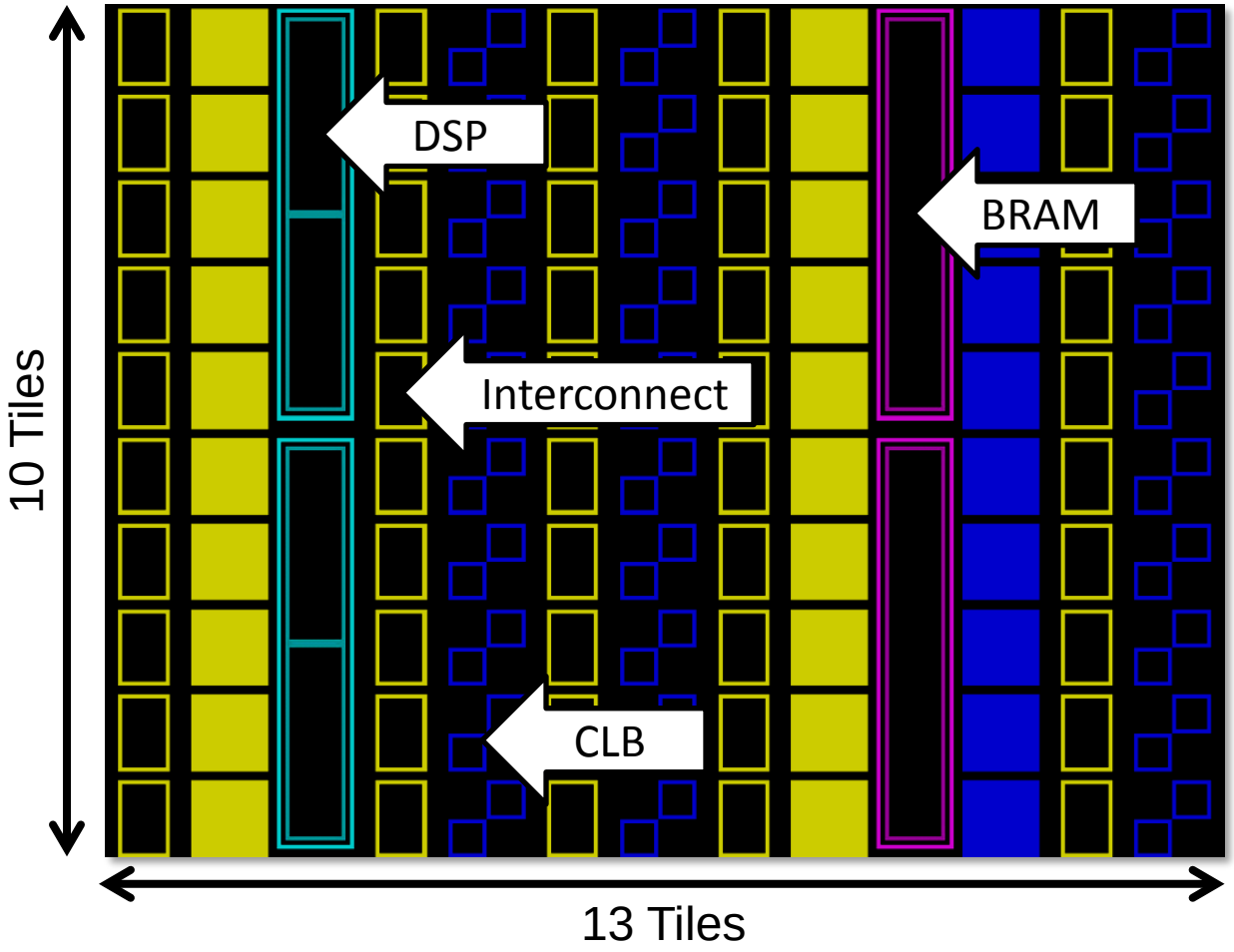
- Ever-larger FPGA devices increase placement problem difficulty
- Vendors suggest *floor-planning* to guide placement
- A *floor-plan* is a map of design submodules to physical FPGA regions



How to Floor-plan?

- What aspect ratios are best for submodules that comprise the floor-plan?
- How much area should be allocated for a submodule?
- What impact do area constraints have on the maximum clock rate for a submodule?
- What guidelines should be followed when assigning submodules to physical locations on the FPGA?

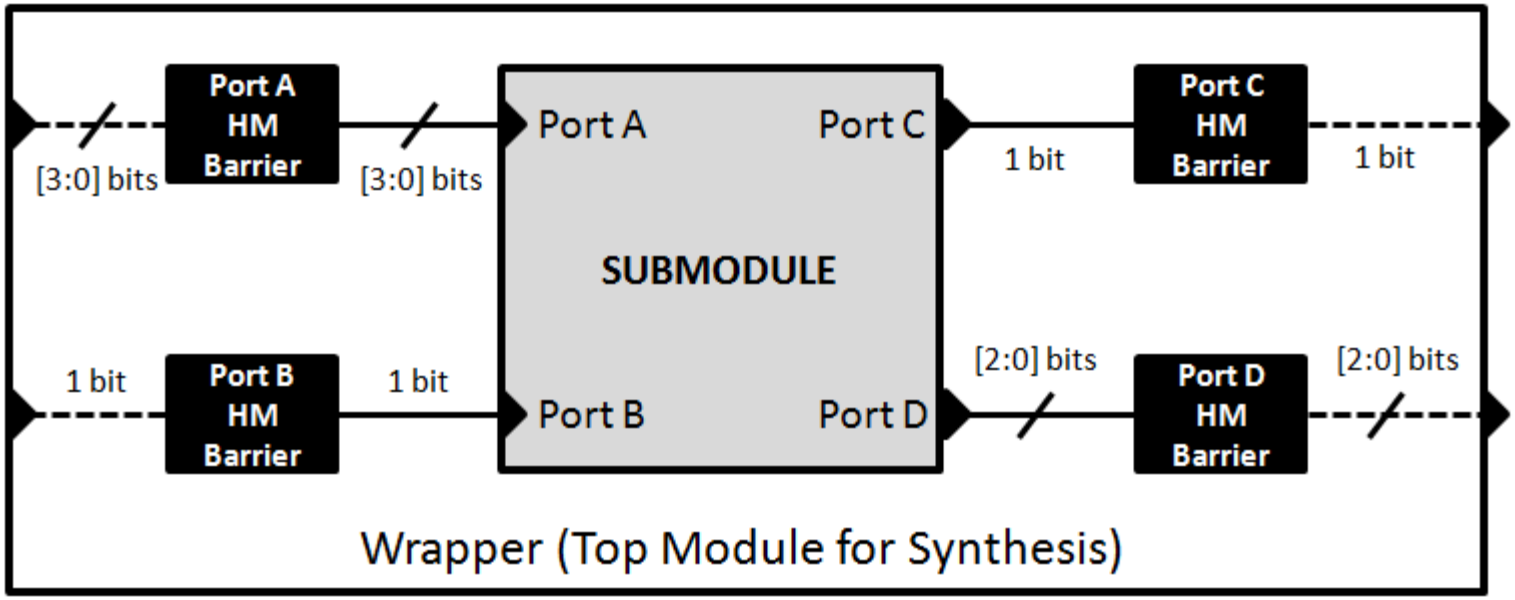
Xilinx Device Tiles



VIEWED WITH

RAPID SMITH

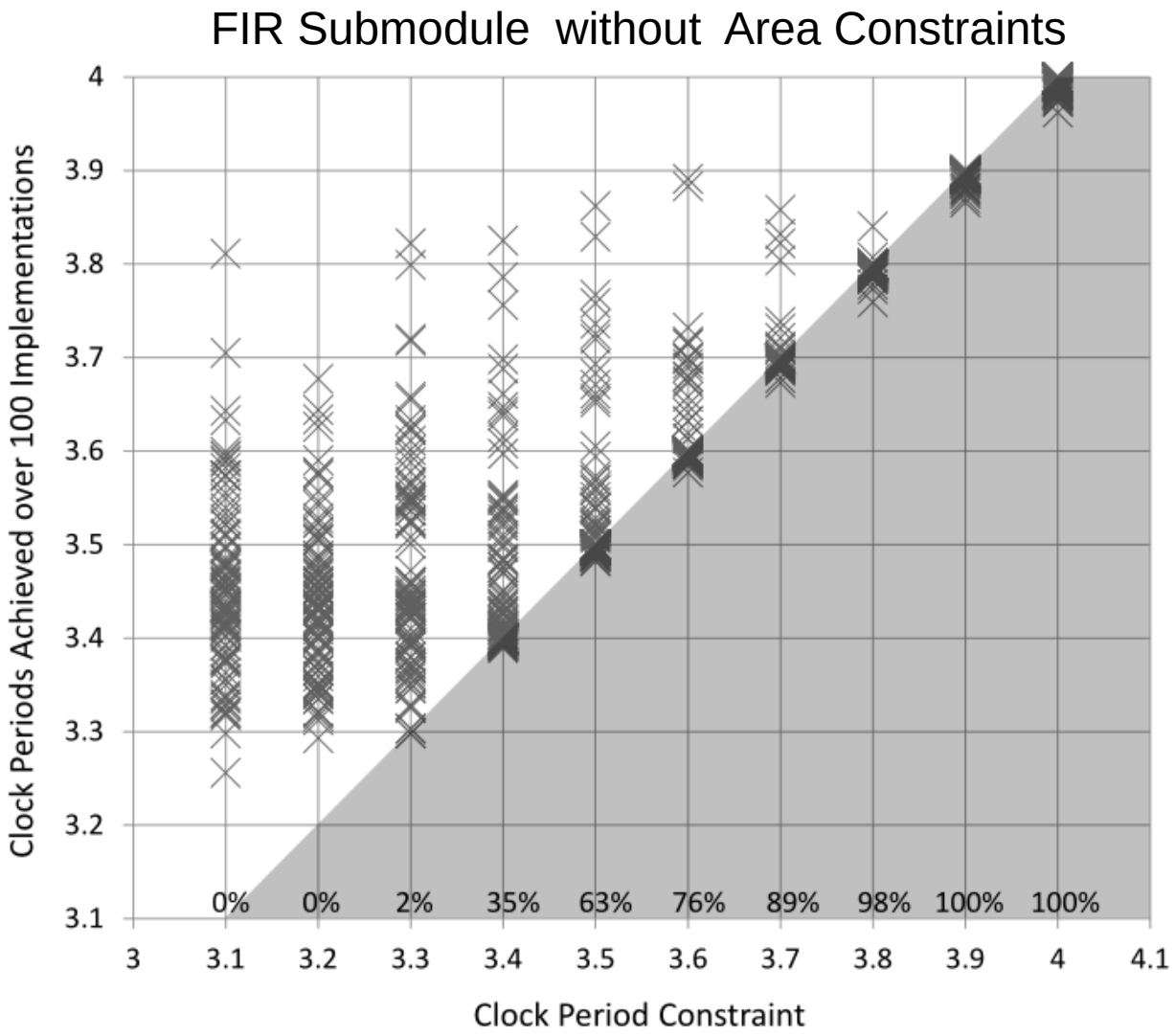
Independent Submodule Implementation



Submodule Resource Requirements

Submodule	Logic LUTs	Memory LUTs	Registers	BRAMs	DSPs
FFT	2574	571	4001	5	12
FIR	3106	36	7376	0	100
FP	13270	450	21584	12	40
Microblaze	1395	84	1443	0	3
Mult	362	23	466	0	0
Picoblaze	113	34	135	0	0

Submodule Baseline Clock Constraints



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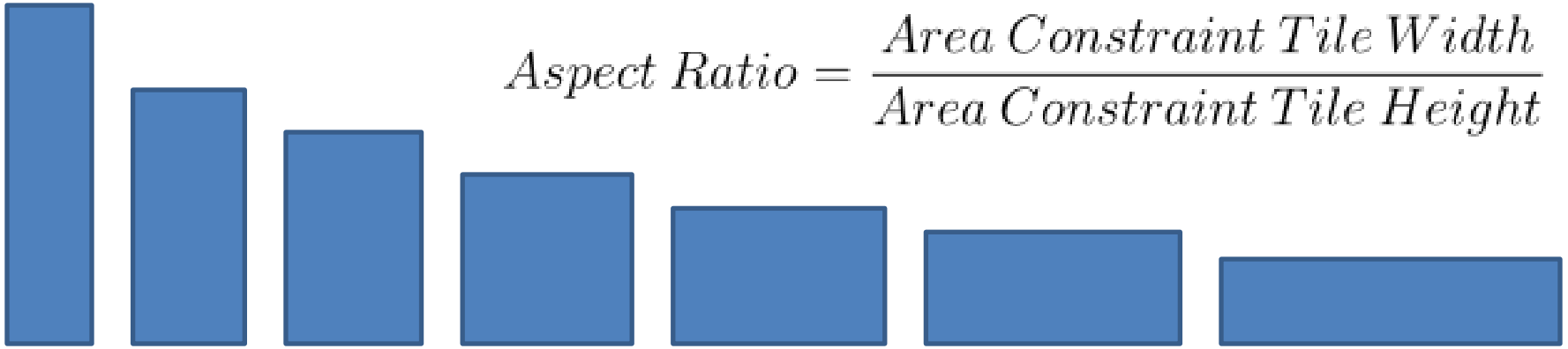
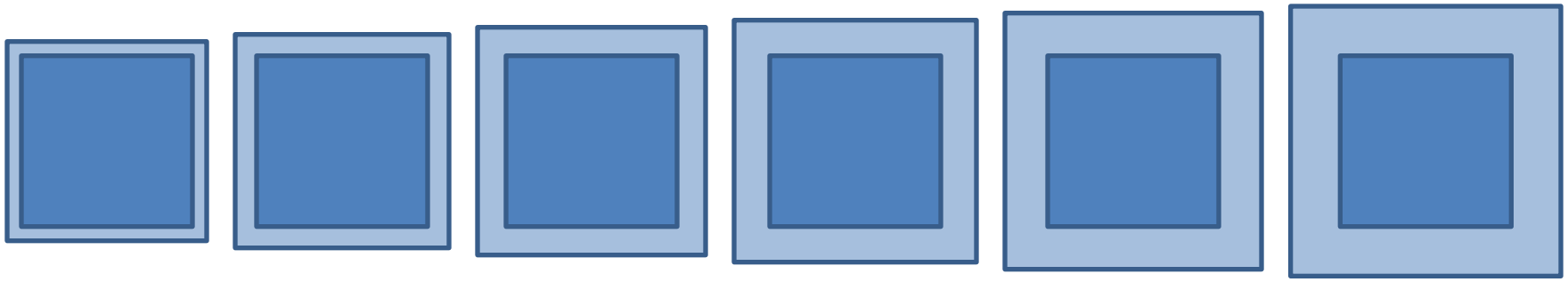
Area Constraint Variation



$$Aspect\ Ratio = \frac{Area\ Constraint\ Tile\ Width}{Area\ Constraint\ Tile\ Height}$$

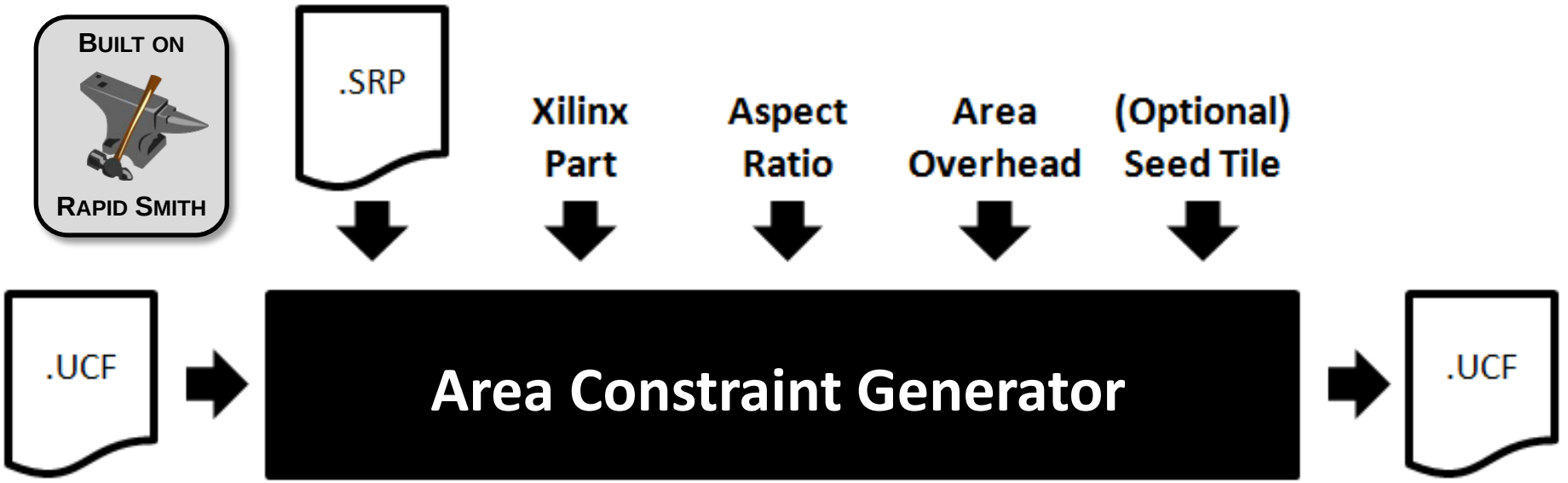
$$Area\ Overhead\ \% = \left(\frac{Resources\ Within\ Area}{Estimated\ Resources\ Required} - 1 \right) \times 100$$



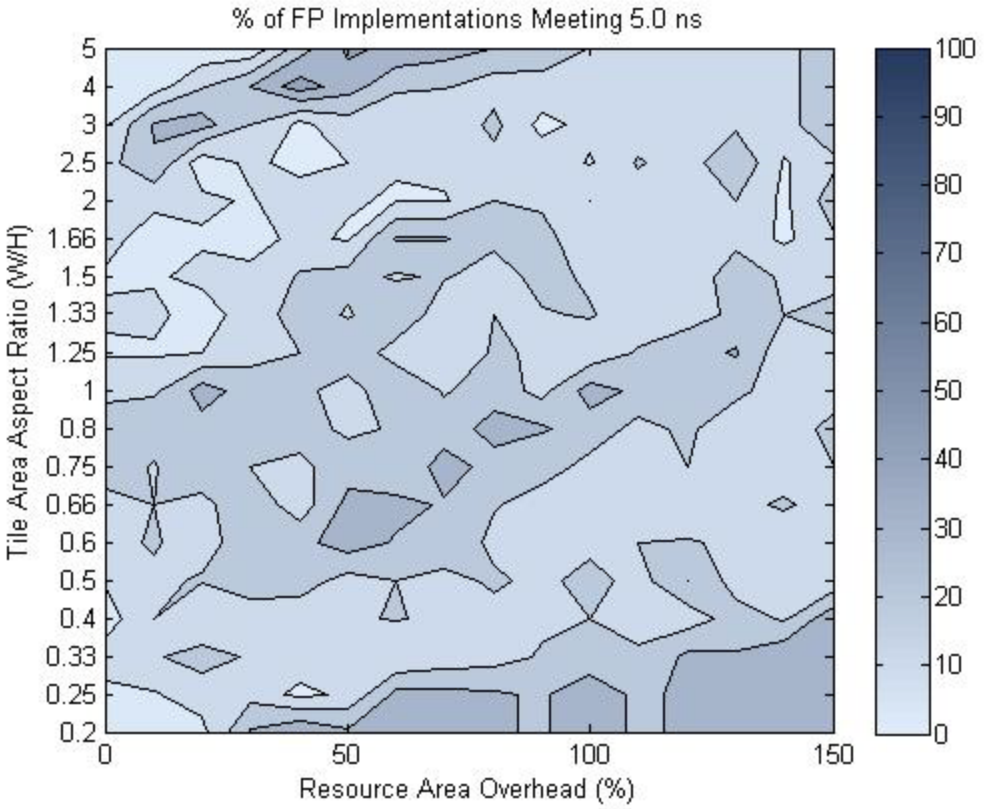
100,000's of Implementations

For each submodule:

- Aspect Ratio: all ratios from ints 1 to 5.
- Area Overhead: 0-150%, 10% step
- Seeds: all MAP seeds (-t [1…100])
- Scripted constraint generation



Submodule Implementation Results



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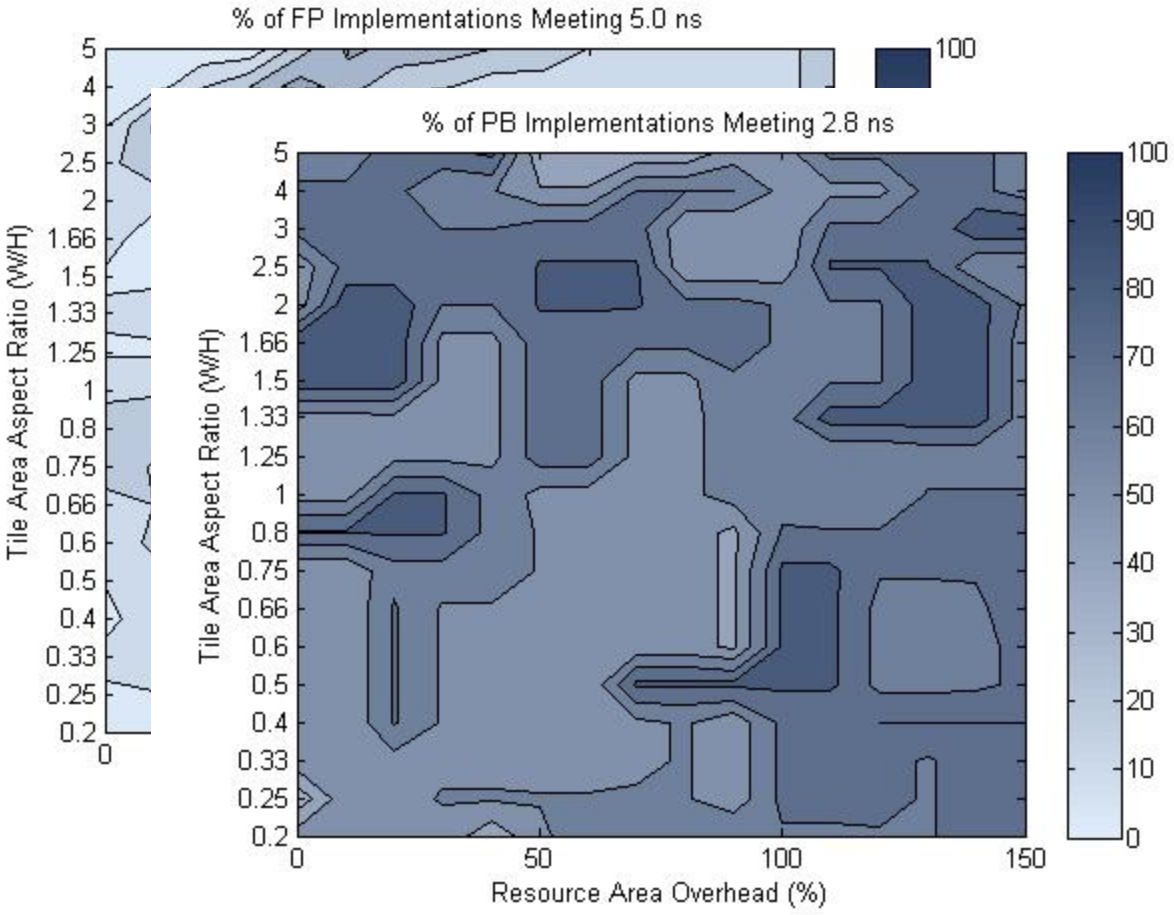

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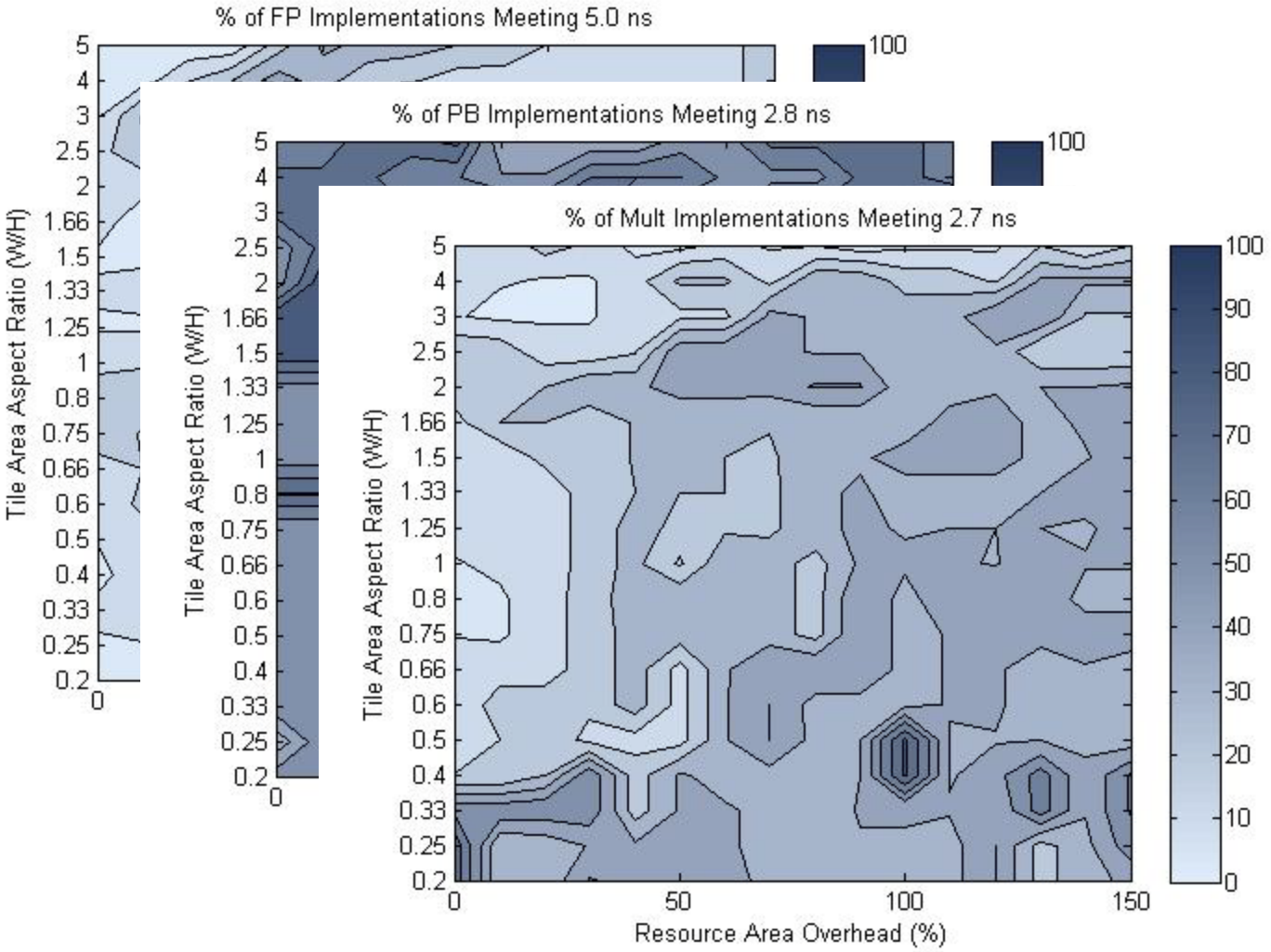

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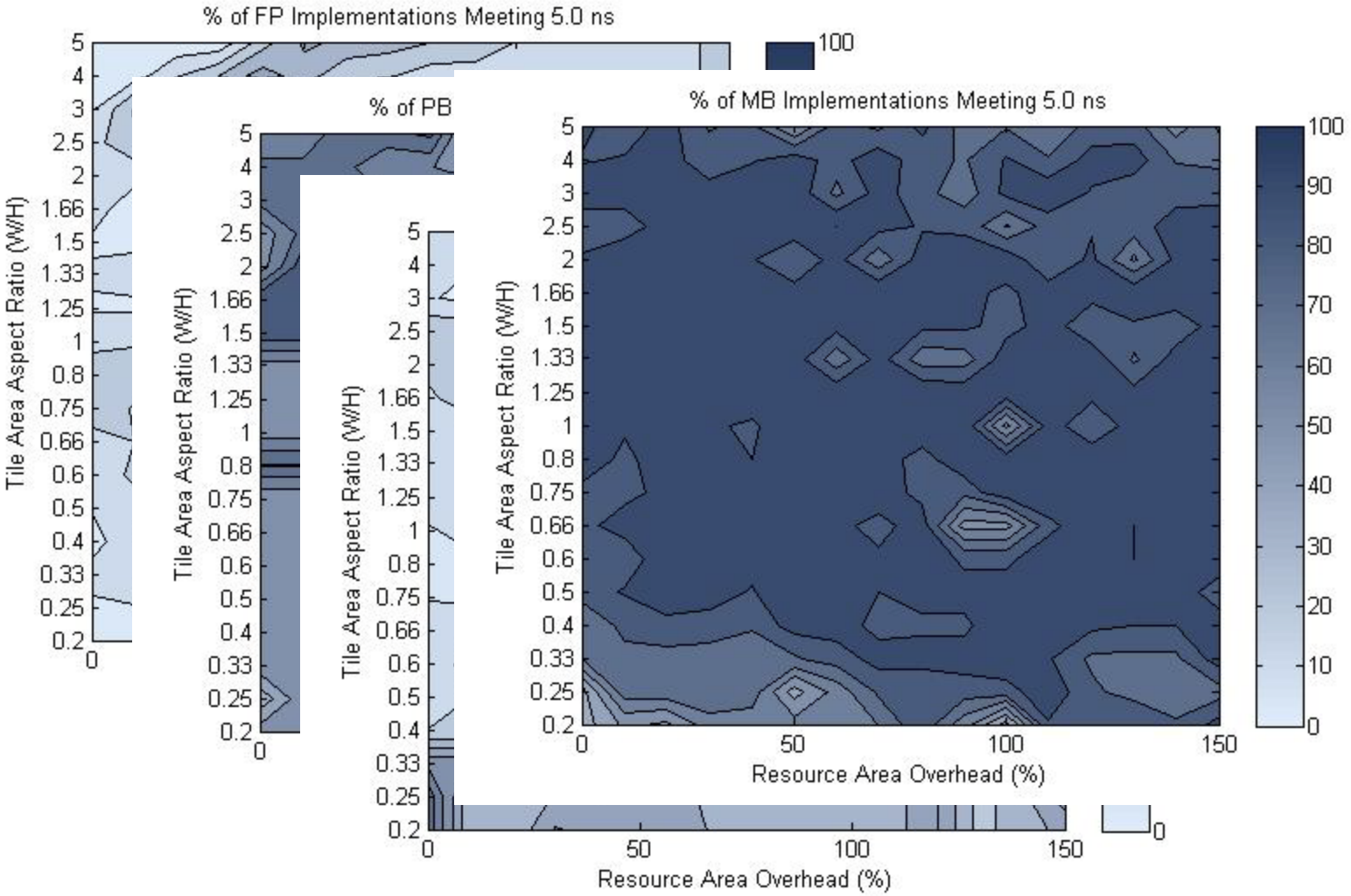

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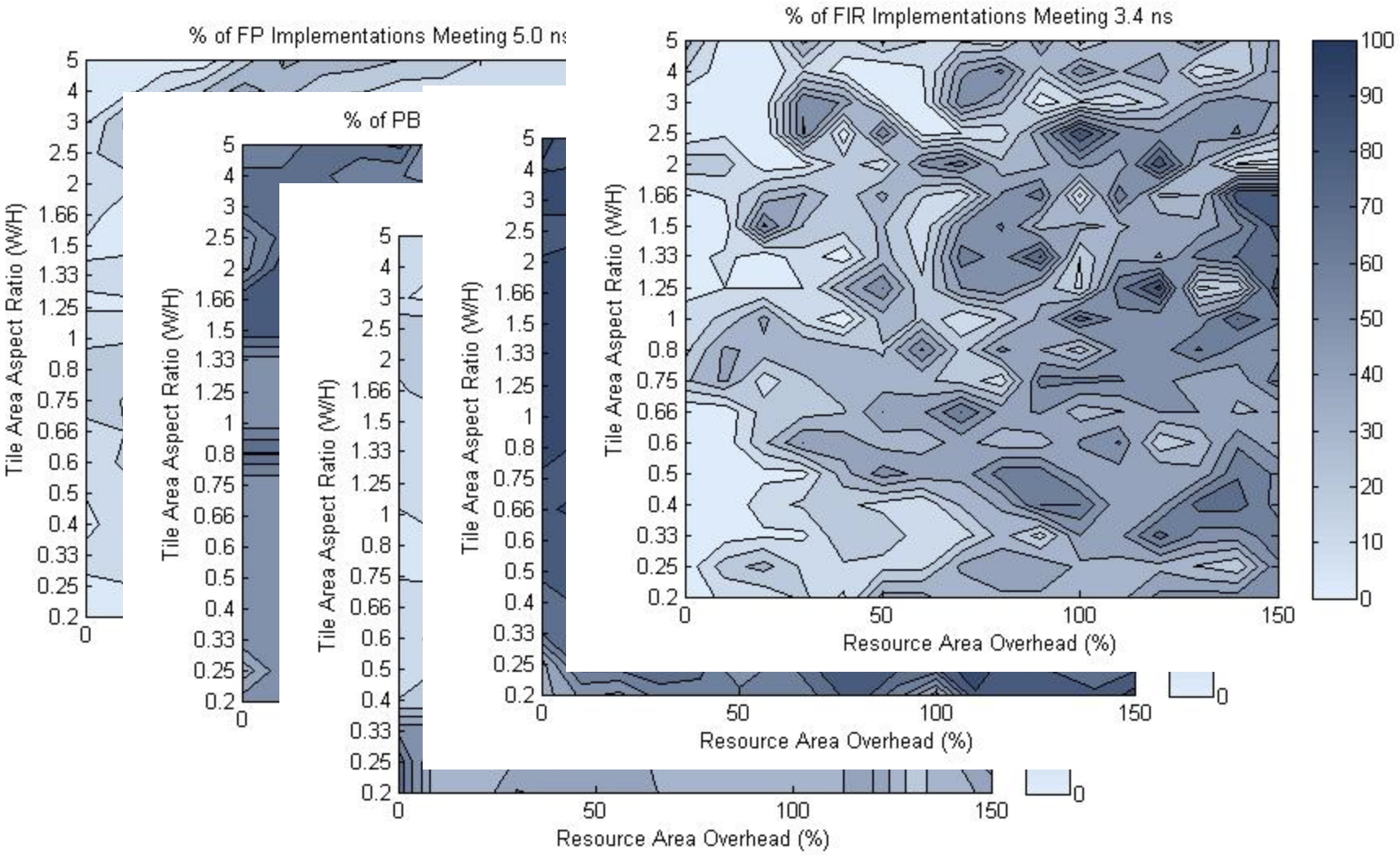

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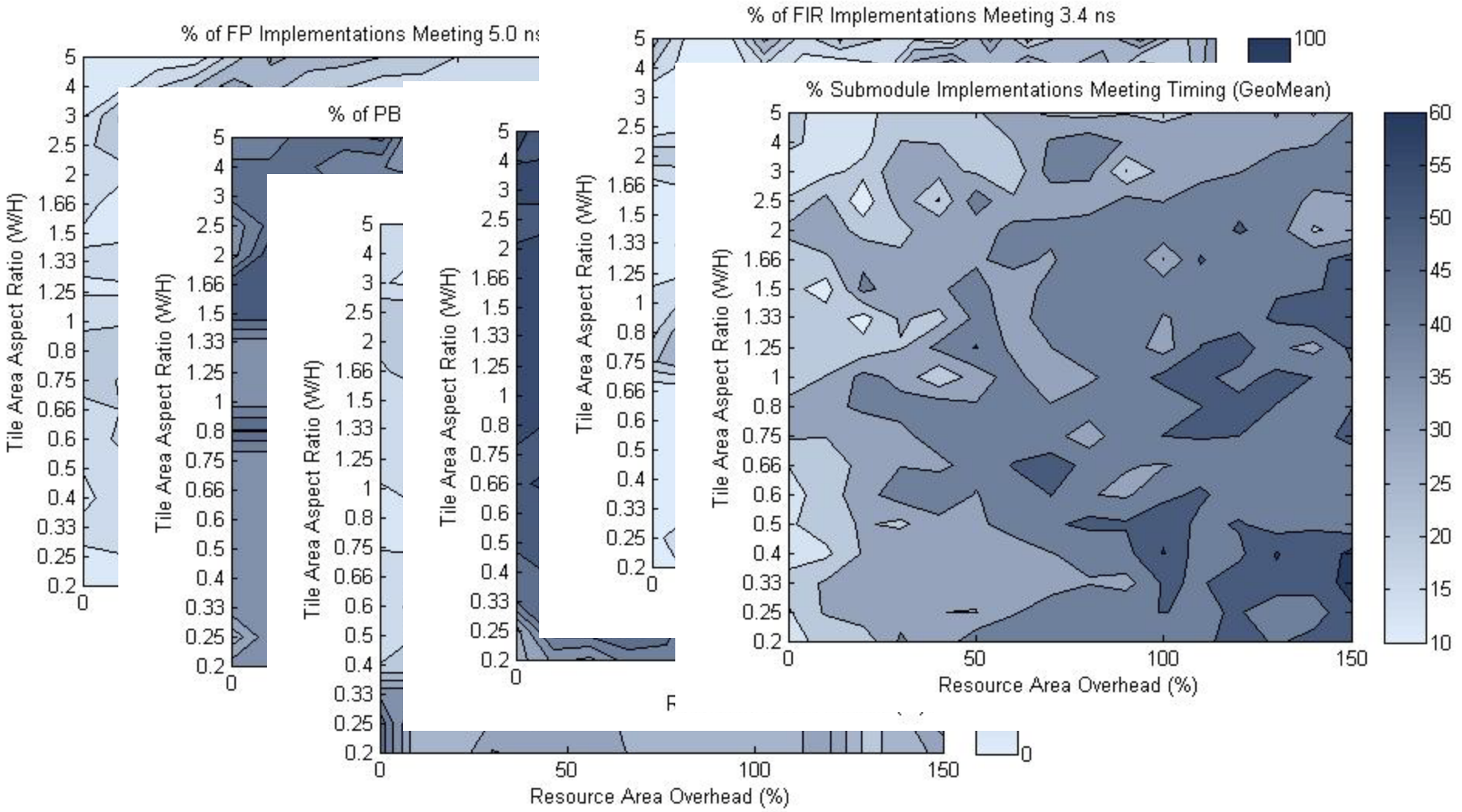

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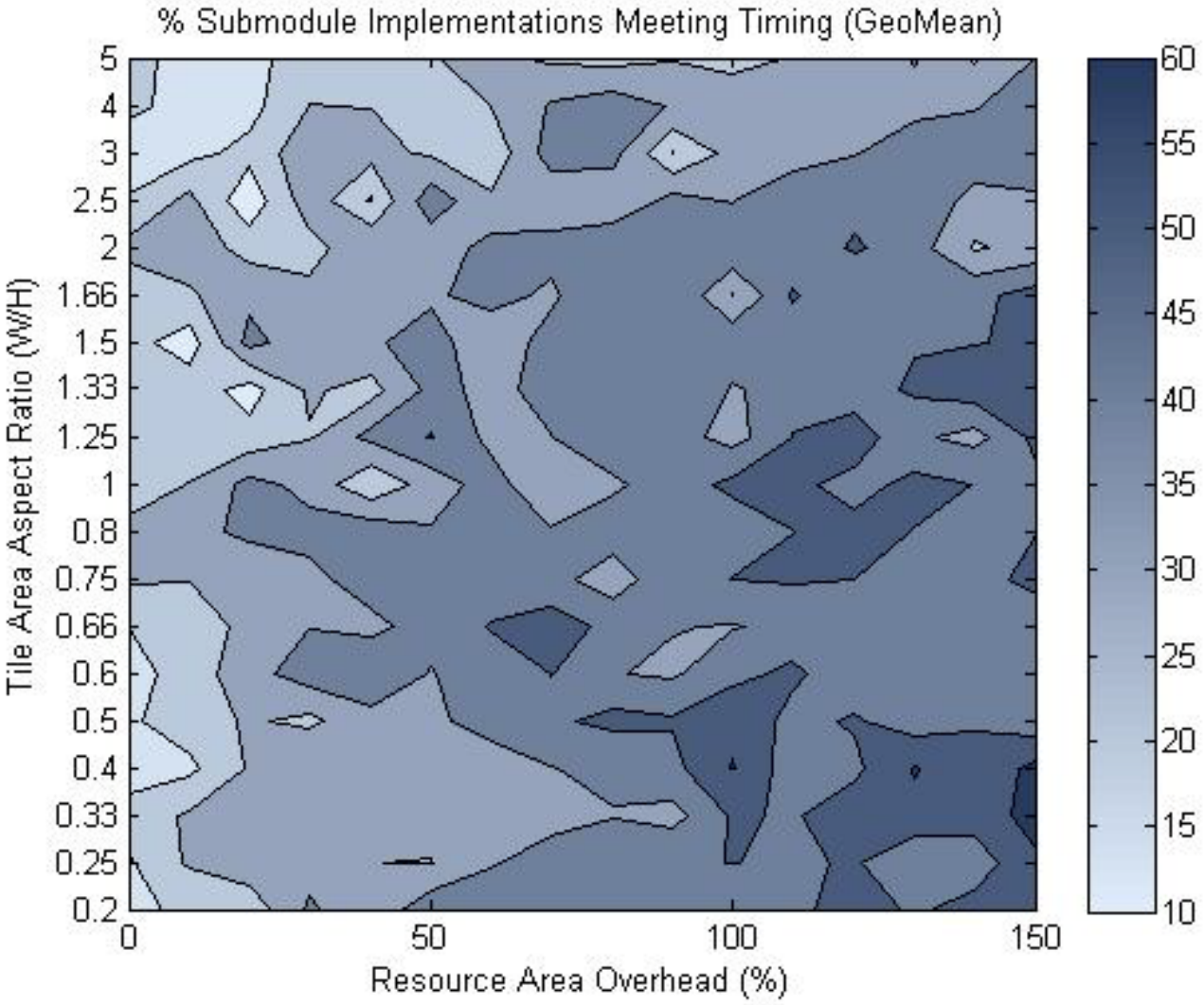
General Results



- Any combination of aspect ratio and area overhead *can* meet timing constraints

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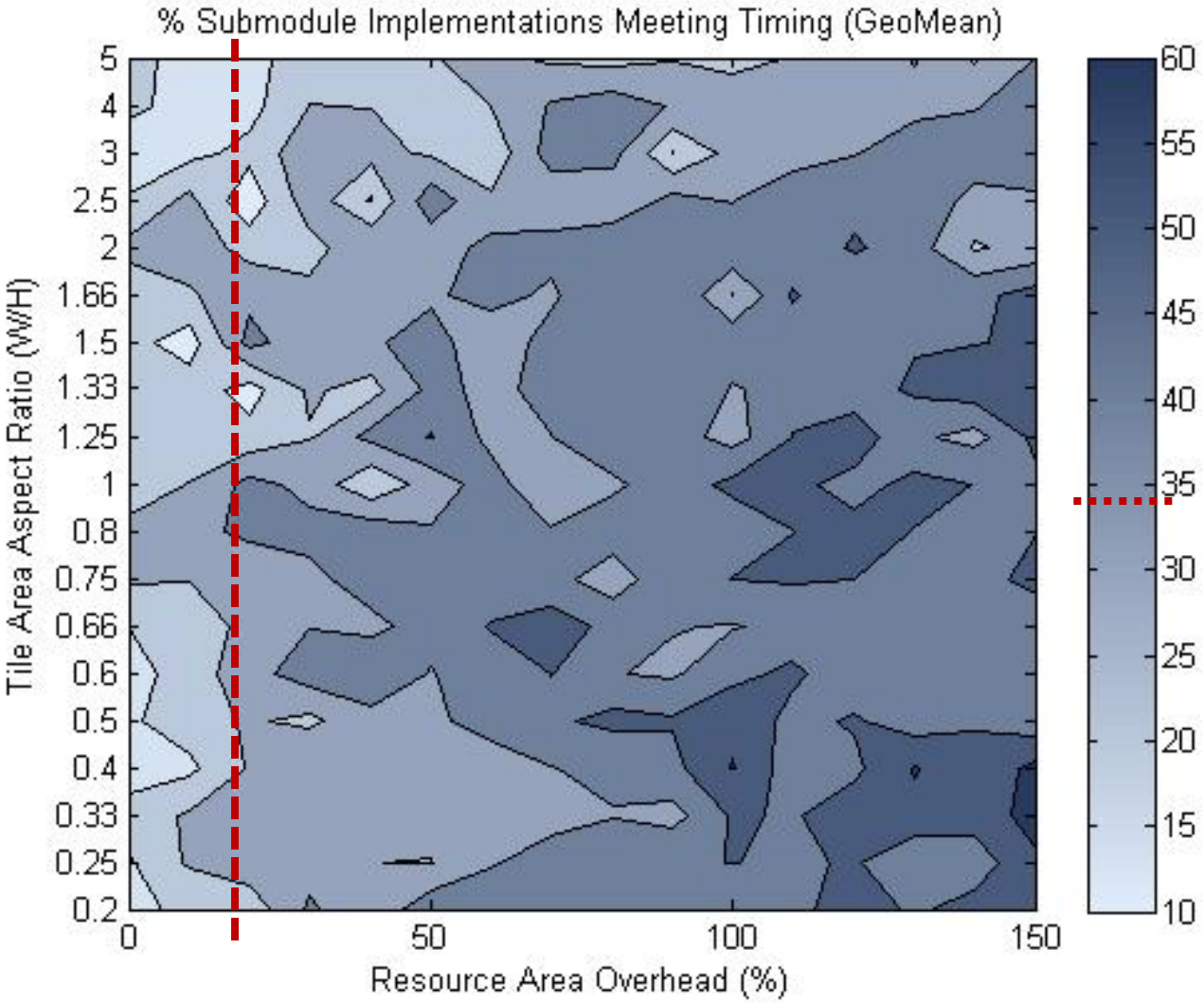

- Any combination of aspect ratio and area overhead *can* meet timing constraints
- Above 20% area overhead, most combinations meet timing at least as often as implementations without area constraints

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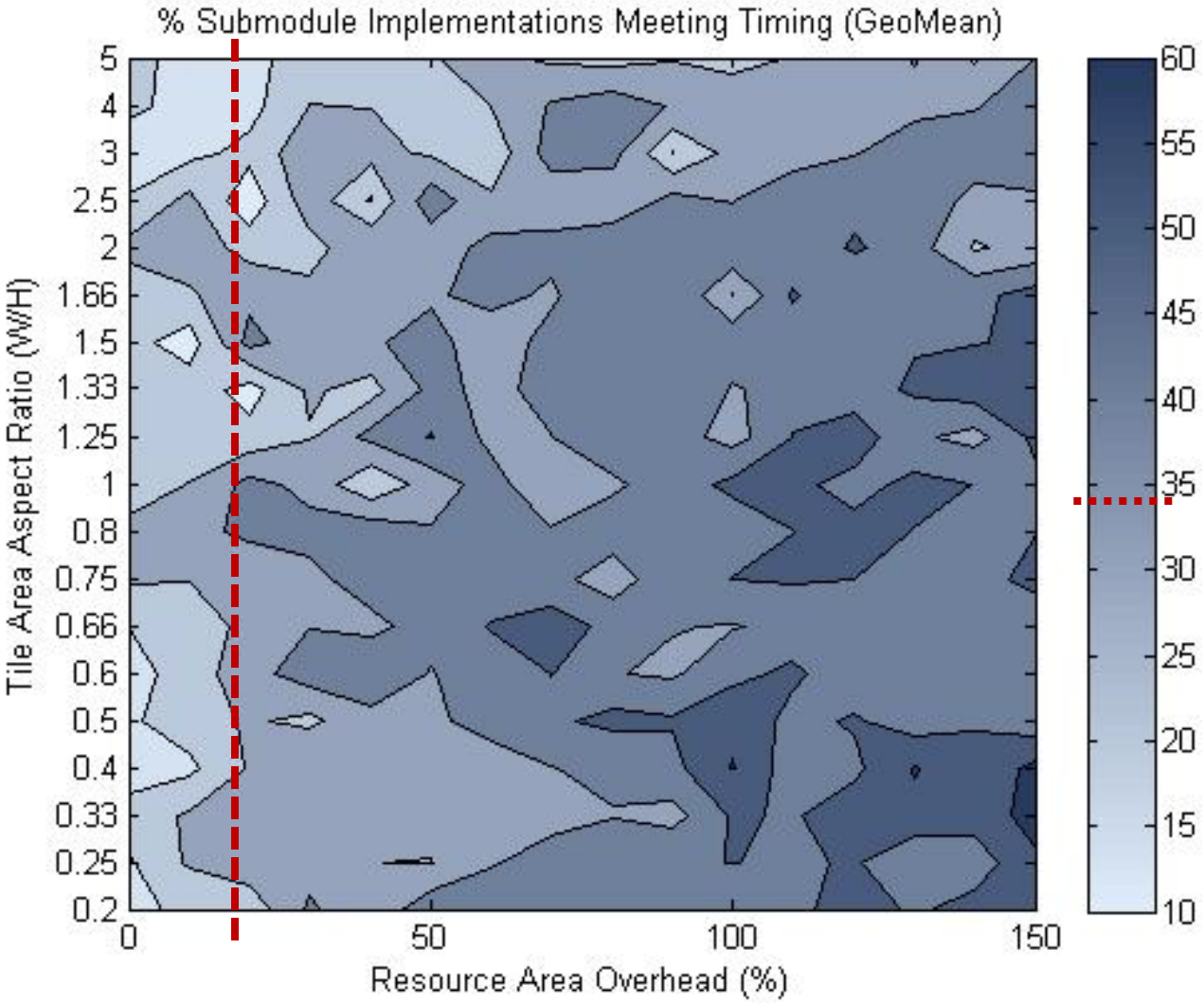
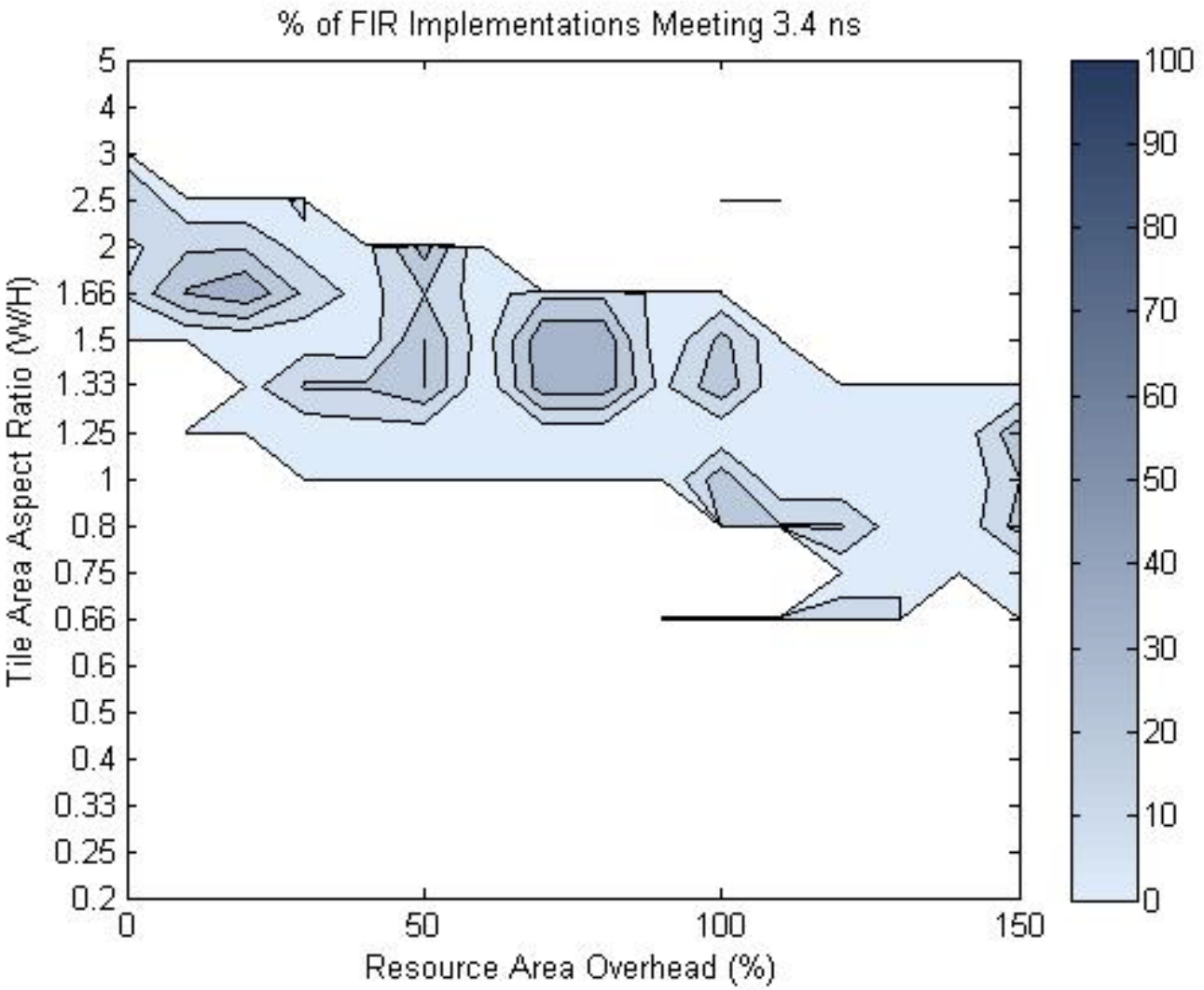


- Any combination of aspect ratio and area overhead *can* meet timing constraints
- Above 20% area overhead, most combinations meet timing at least as often as implementations without area constraints
- At or below 20% area overhead, aspect ratio noticeably impacts results. Moderate aspect ratios preferred.

Exceptional Results



- FIR submodule cannot meet timing at all combinations

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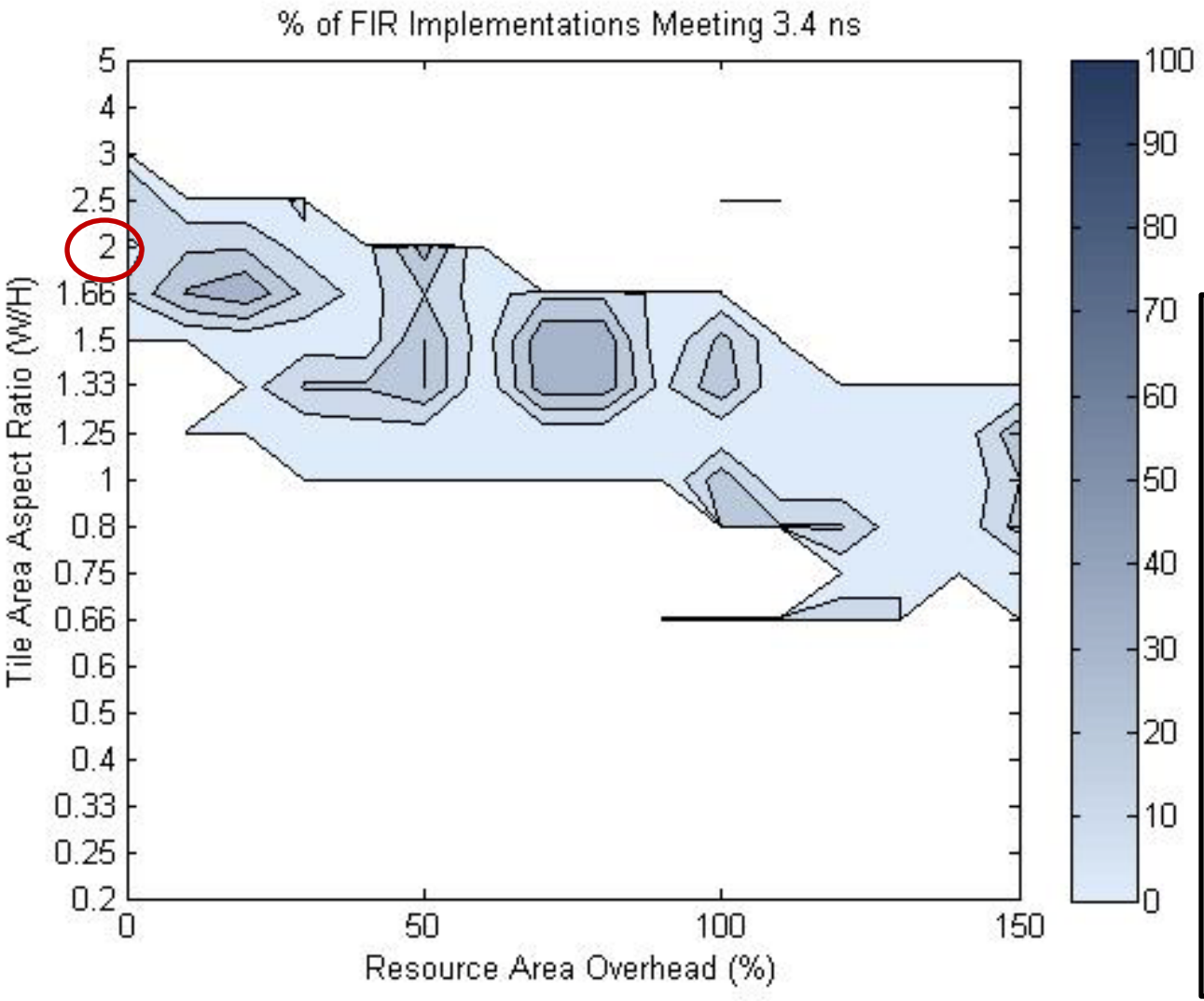
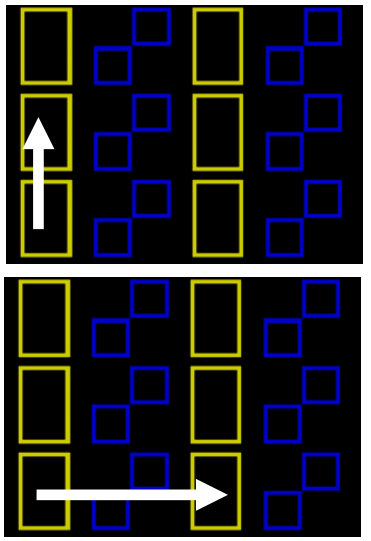


- FIR submodule cannot meet timing at all combinations
- Prefers 2.0 aspect ratio

Equivalent Wire Delays

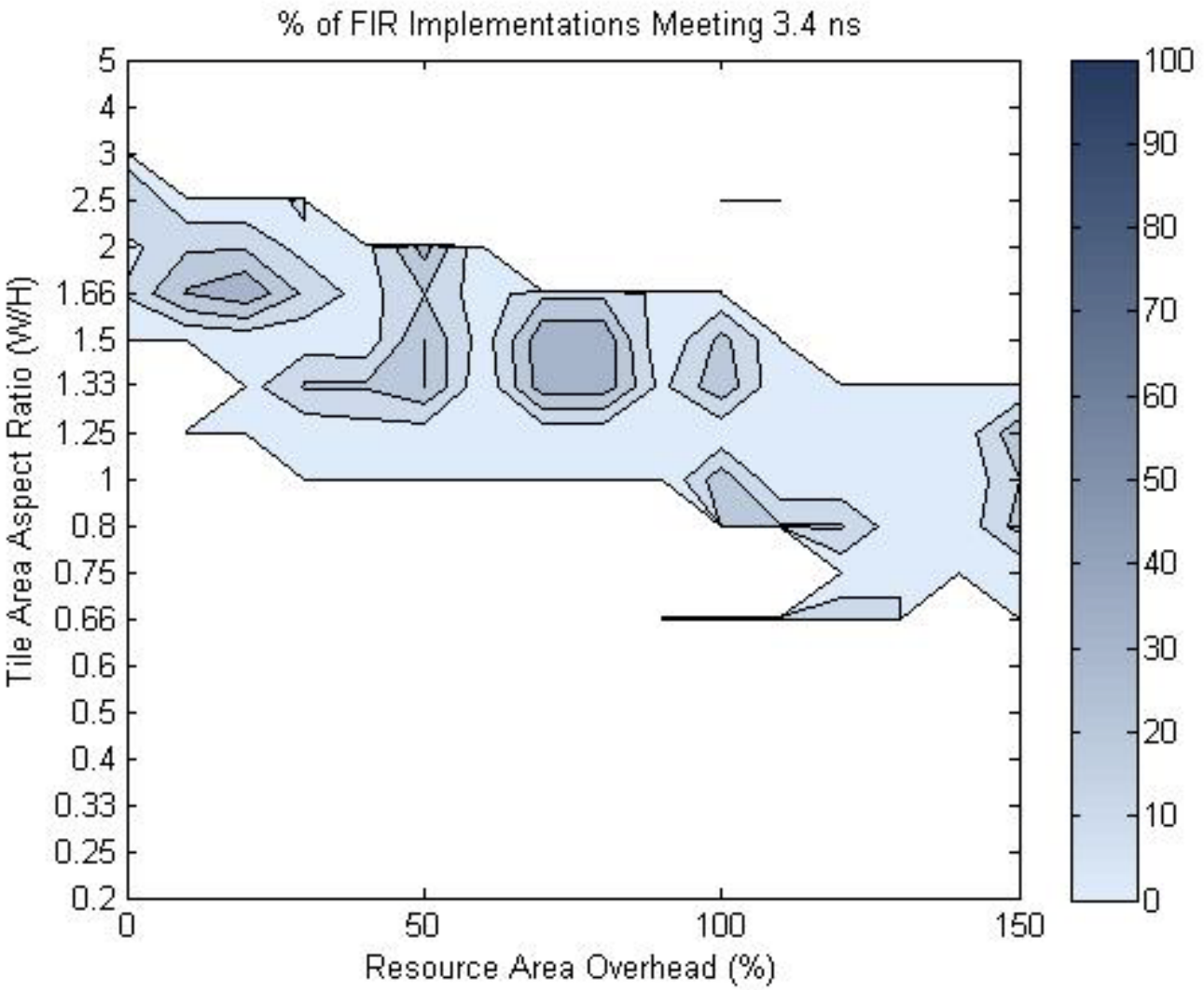


One Vertical Tile Hop

Two Horizontal Tile Hops

Aspect Ratio = (W/H) = (2/1)
For Minimizing Maximum Wire Delay

Exceptional Results



- FIR submodule cannot meet timing at all combinations
- Prefers 2.0 aspect ratio
- Area Constraints crossing the central clock column are troublesome

Submodule Floor-planning Guidelines

- Area constraints do not prevent a submodule from meeting F_{max}.
- Resource area overhead should be greater than 20%.
- Tile aspect ratio is less important, but 2.0 minimizes maximum wire delay.
- Area constraints should not cross the central clock column.

Future Work

- System Designs
  - *Can we draw the same conclusions when we use hard macros in larger systems?*
  - *What is the impact of routing spill-over in system designs?*