

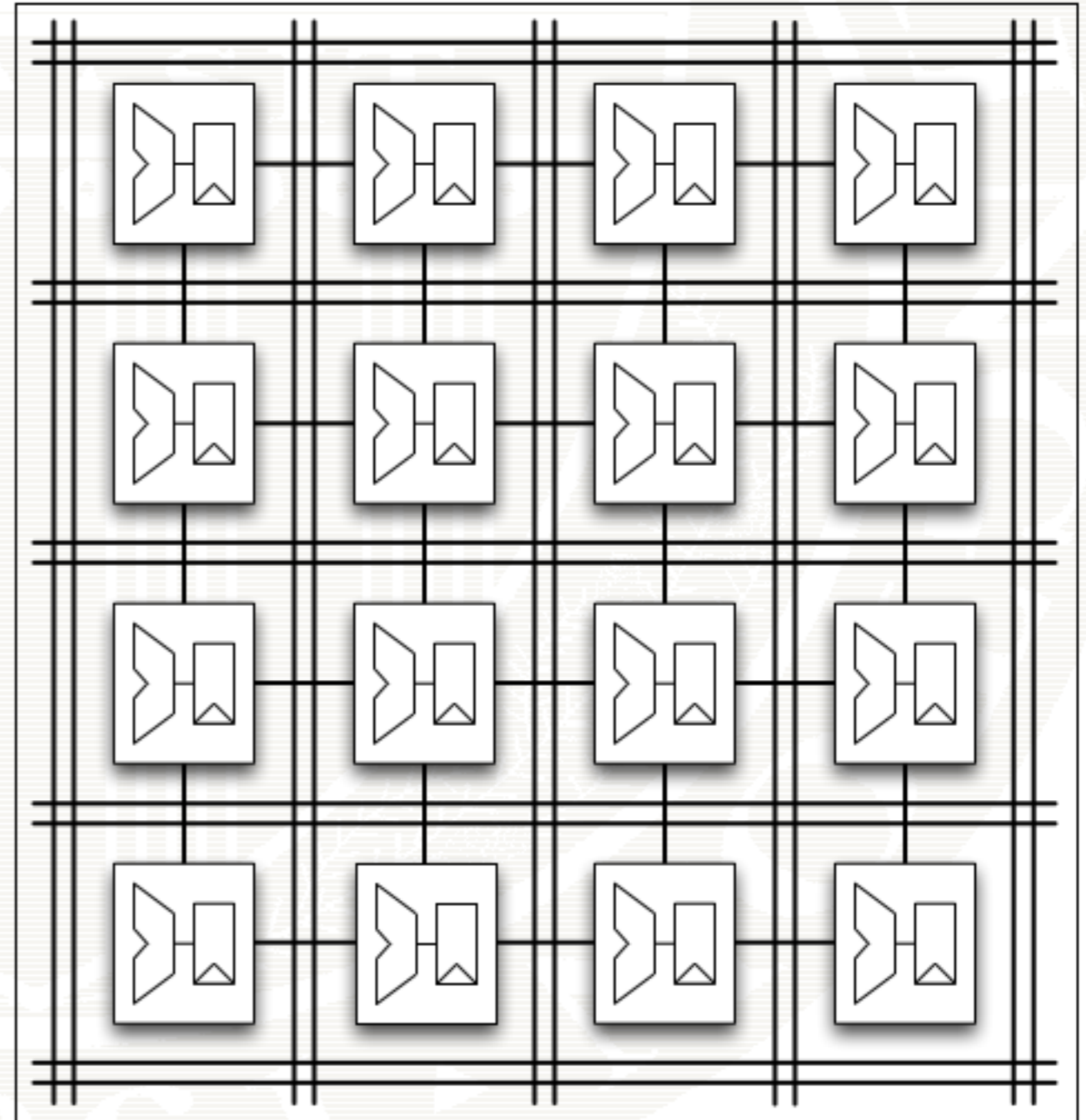
Multi-kernel Floorplanning for Enhanced CGRAs



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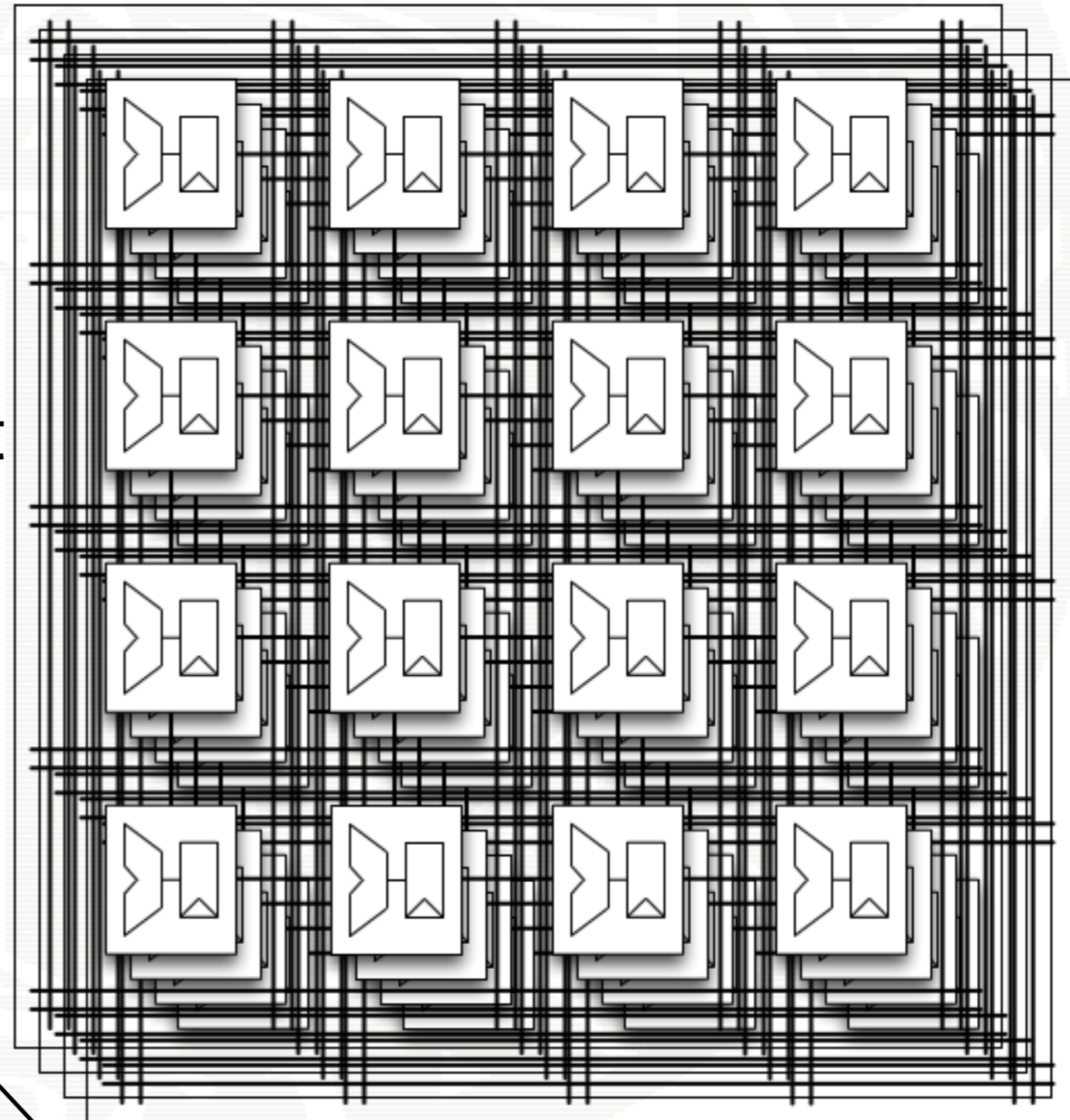
Coarse-Grained Reconfigurable Architectures

- Lots of ALUs
- Word oriented interconnect
- Embedded memory
- Fine grained control
- FPGA style configurability



Time Multiplexing

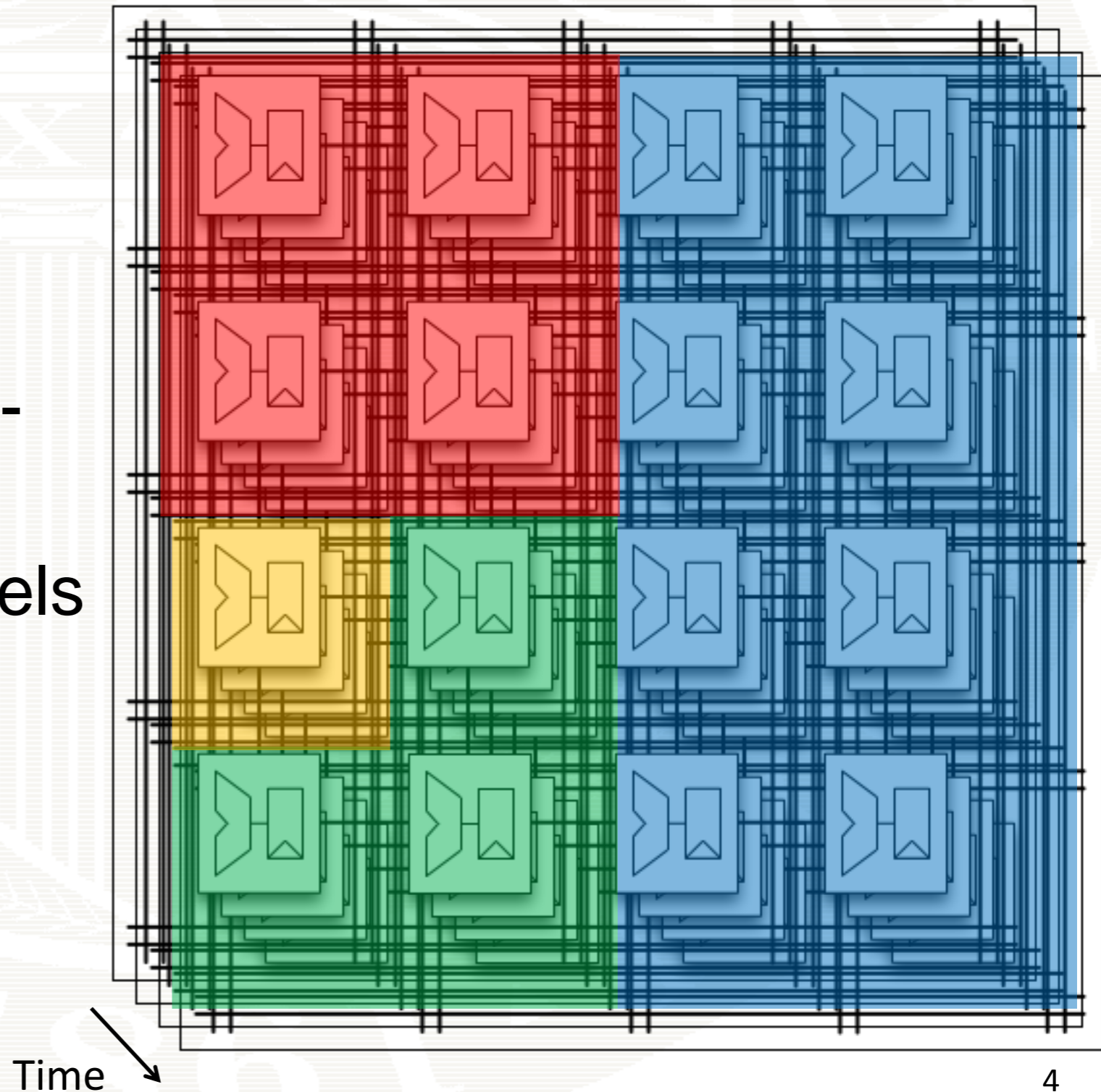
- Small per cycle configurations
- Pipelined applications
- Scheduled interconnect



Time

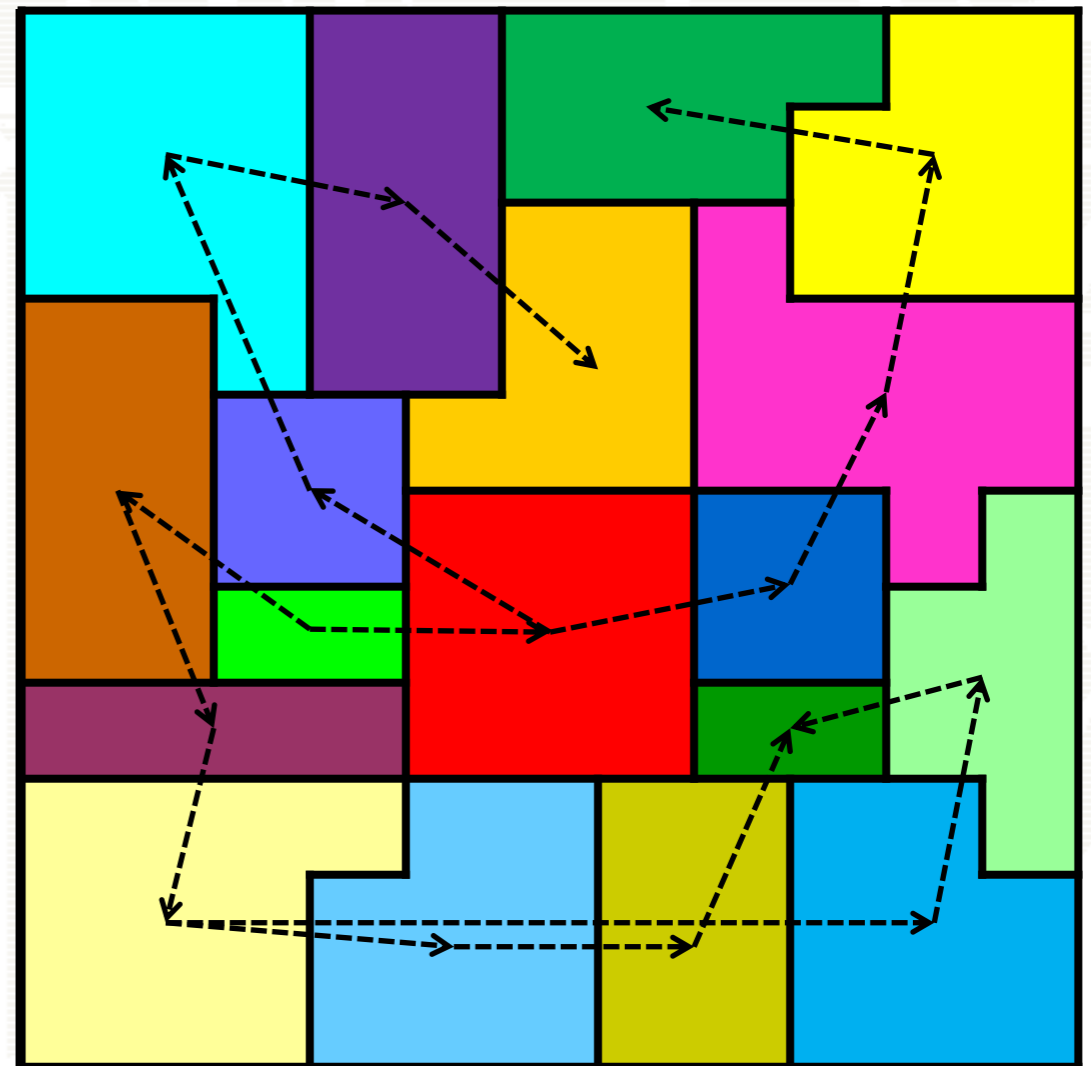
Multiple Kernels

- Physical regions
- Independent control domains
- Flow controlled inter-kernel links
- Composition of kernels



Resource Allocation

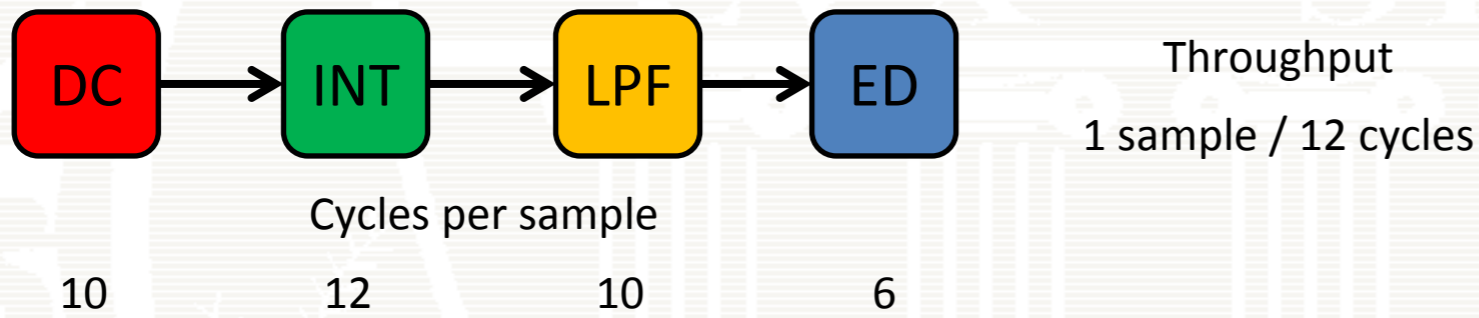
More resources = faster
 Limited total resources
 Maximize throughput



Resource Allocation

Digital camera pipeline example

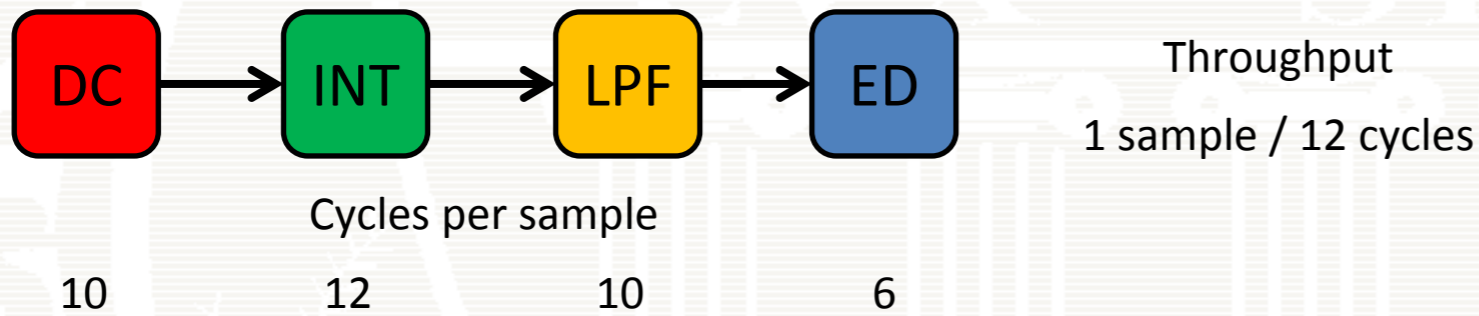
Where do new resources go?



Resource Allocation

Digital camera pipeline example

Where do new resources go?

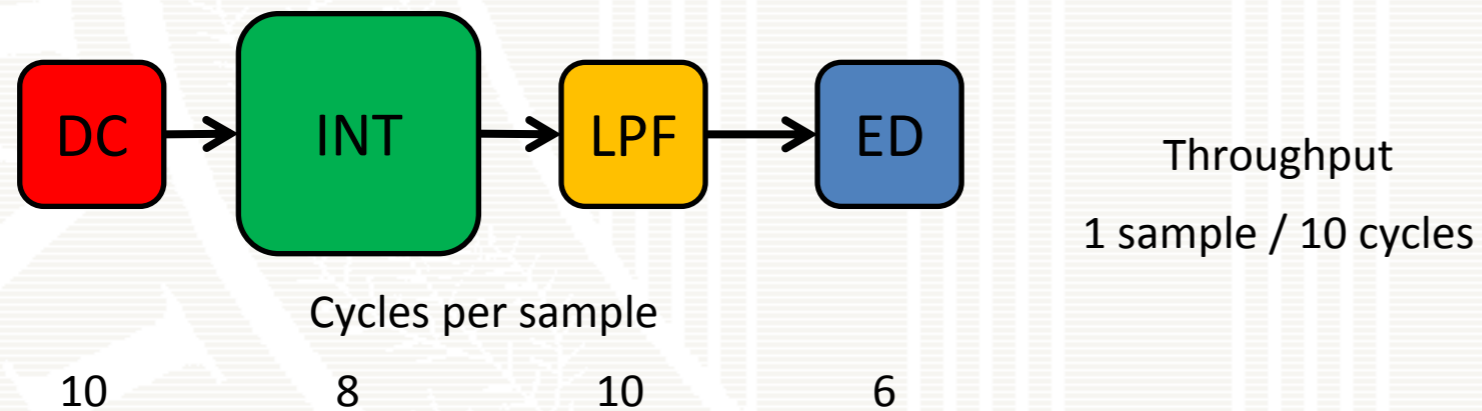
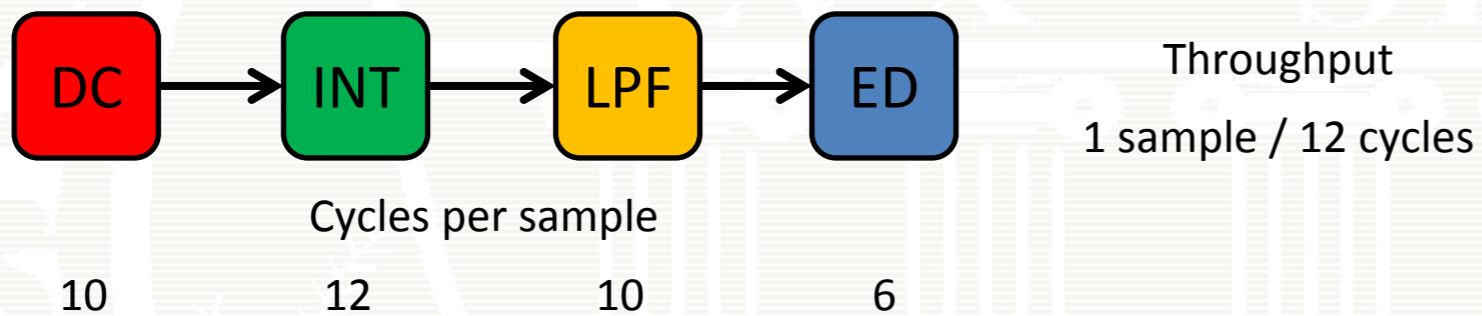


On the slowest kernel

Resource Allocation

Digital camera pipeline example

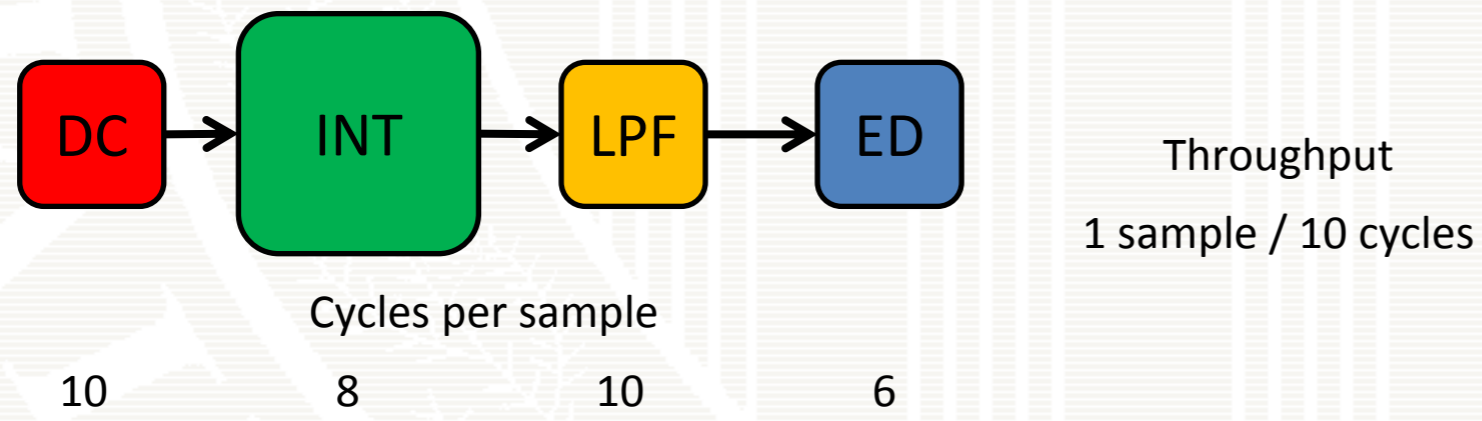
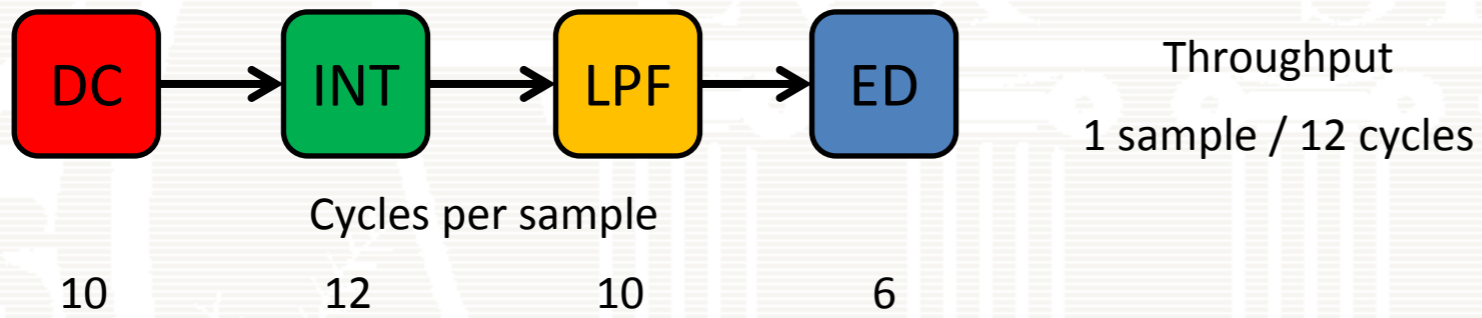
Where do new resources go?



Resource Allocation

Digital camera pipeline example

Where do new resources go?

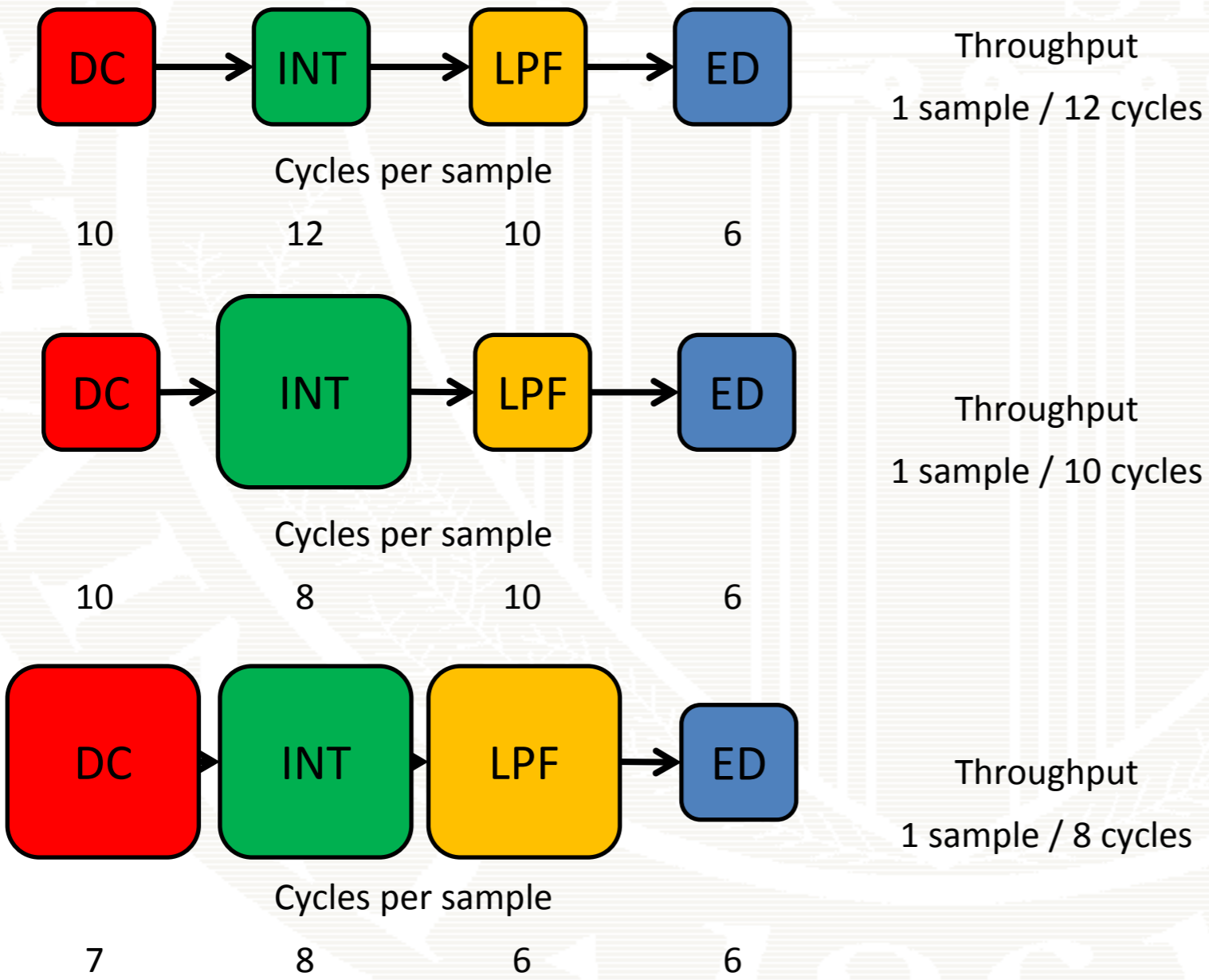


Or set of slowest kernels

Resource Allocation

Digital camera pipeline example

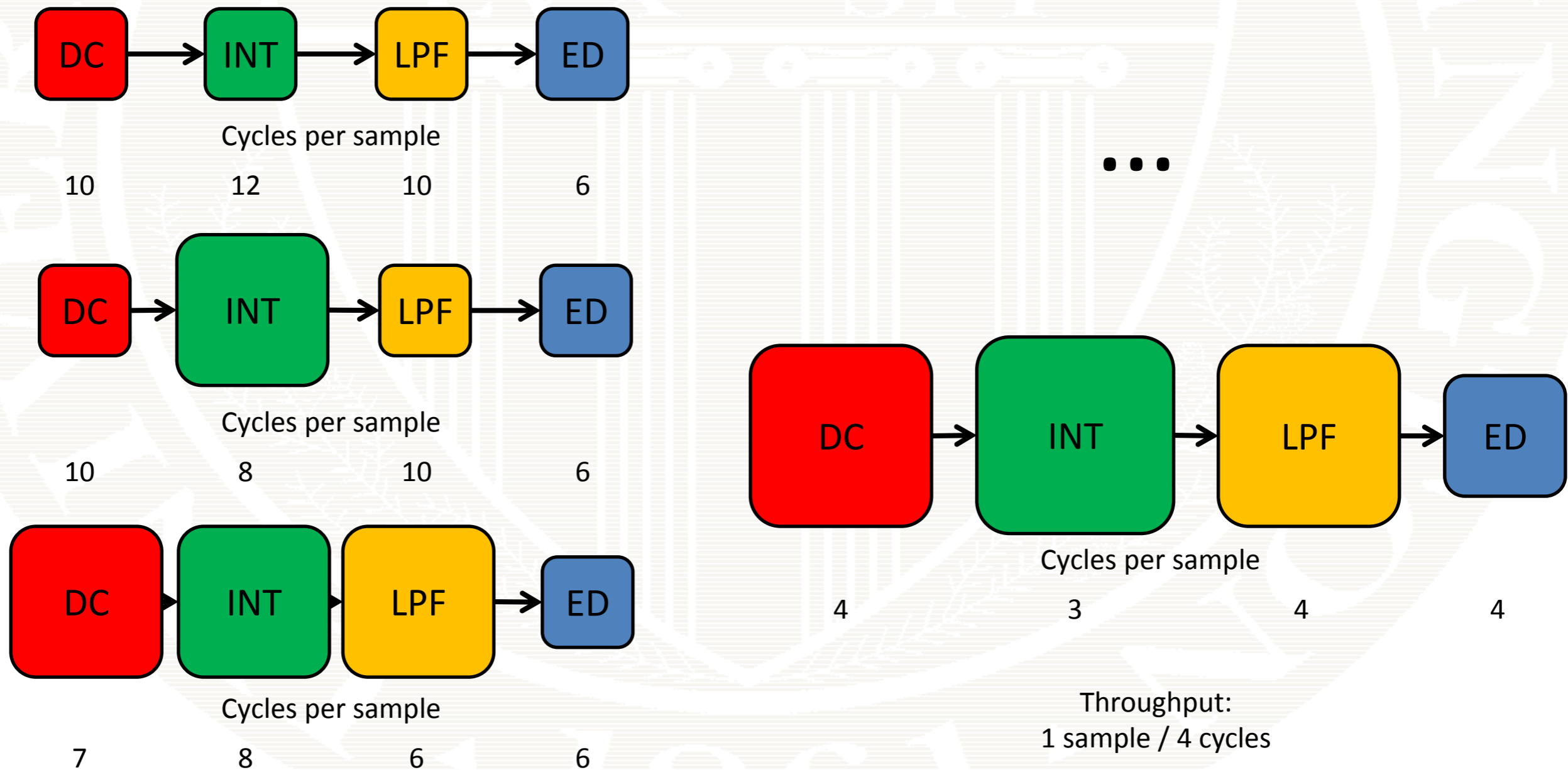
Where do new resources go?



Resource Allocation

Digital camera pipeline example

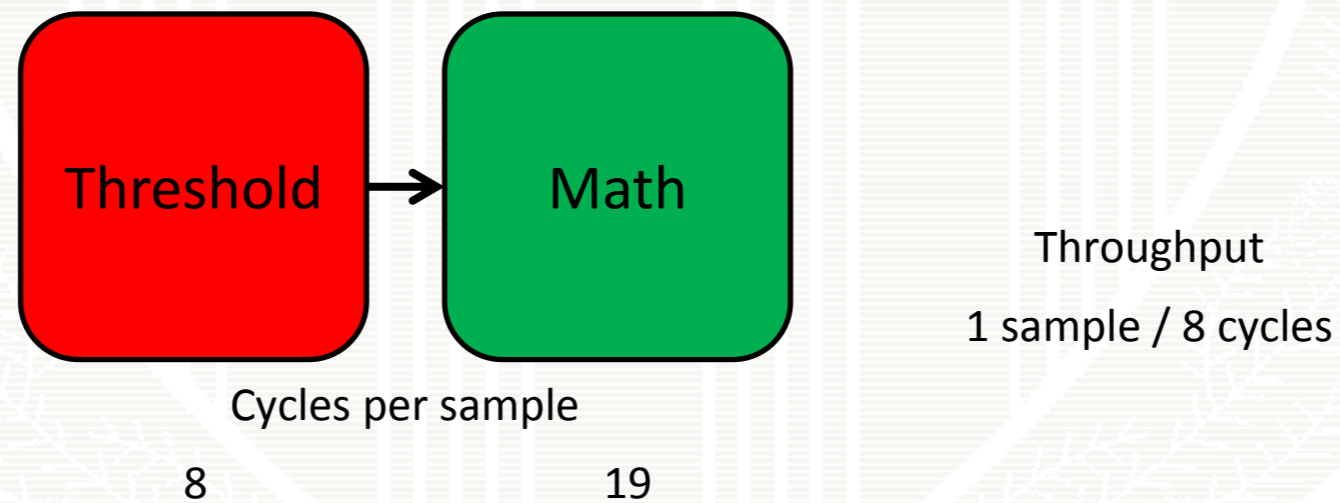
Where do new resources go?



Resource Allocation

PET Event Detection Example

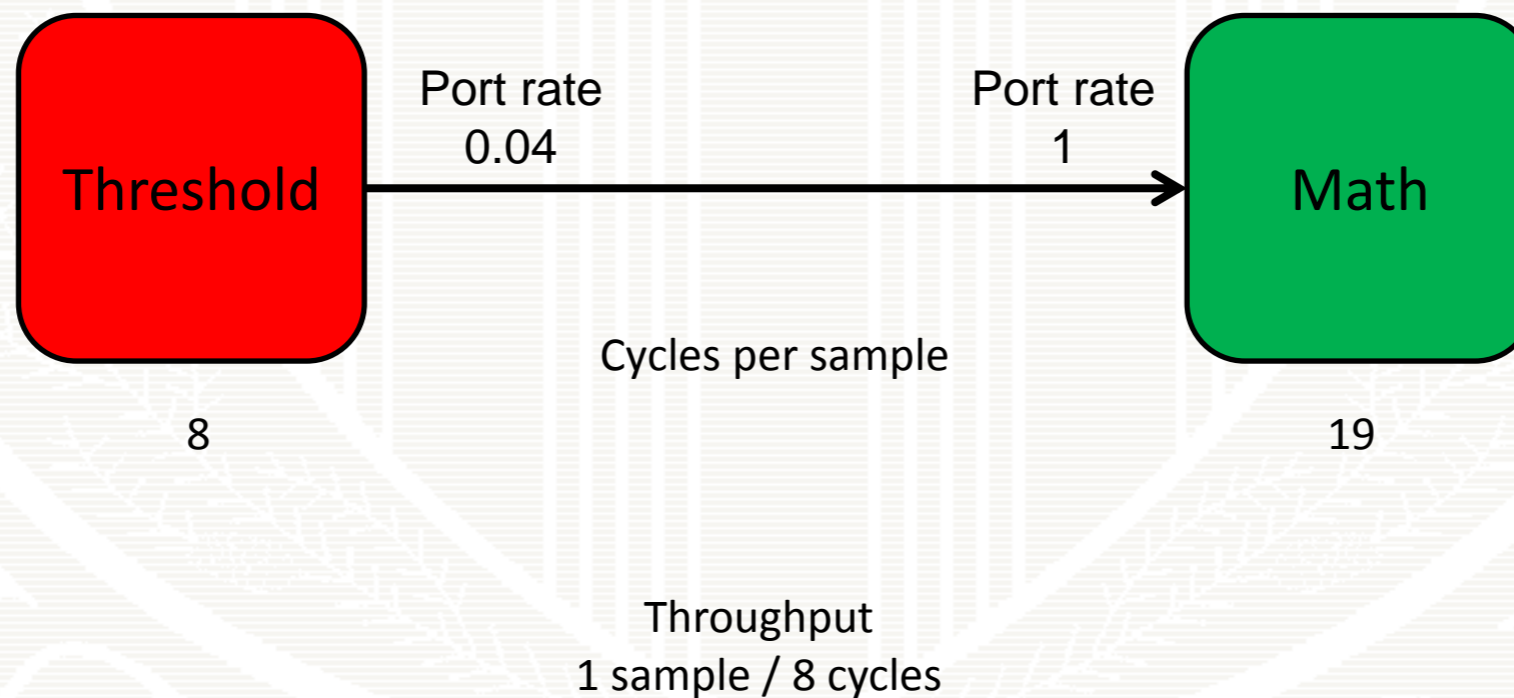
Where do new resources go?



Resource Allocation

PET Event Detection Example

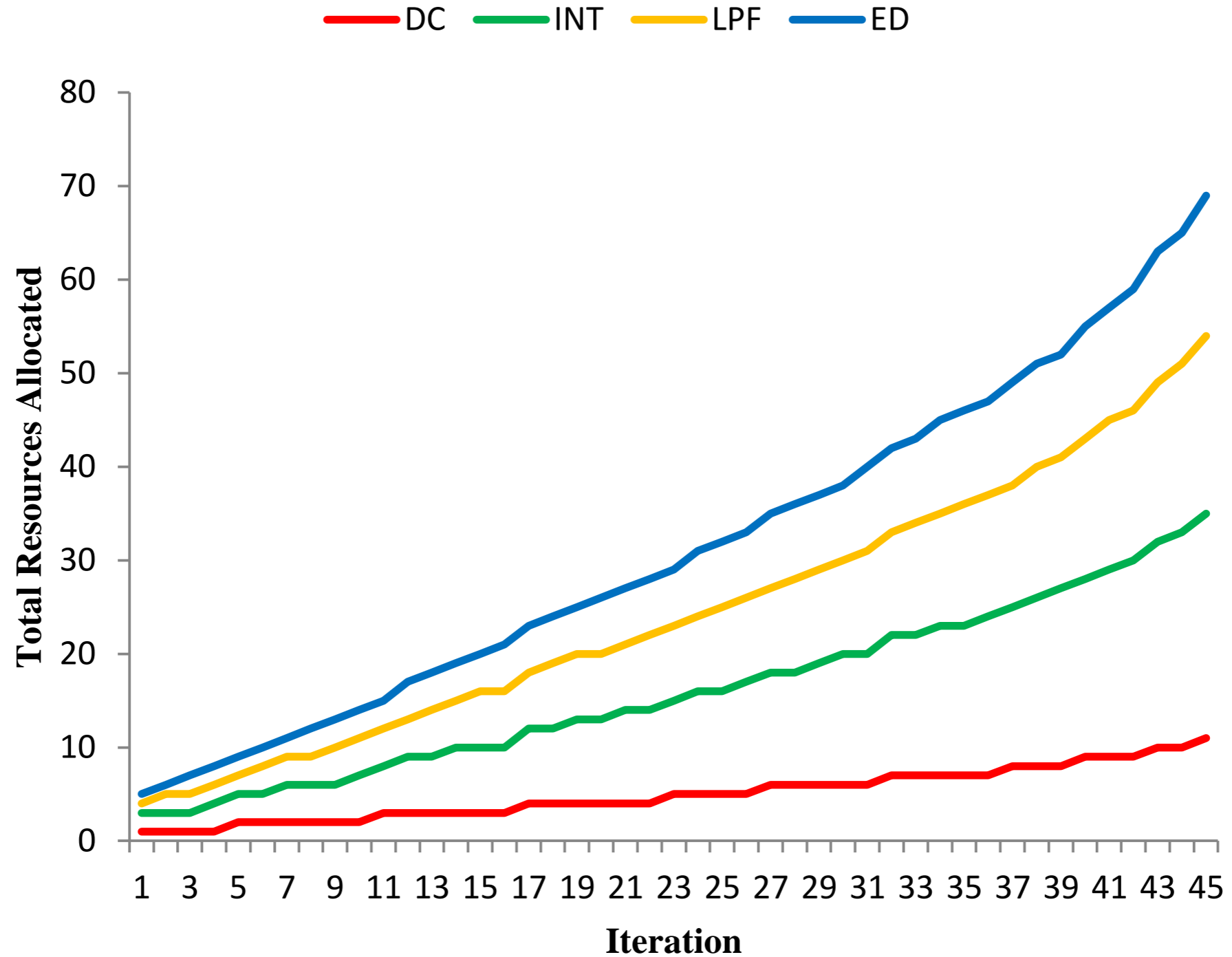
What happened to the slowest kernel?



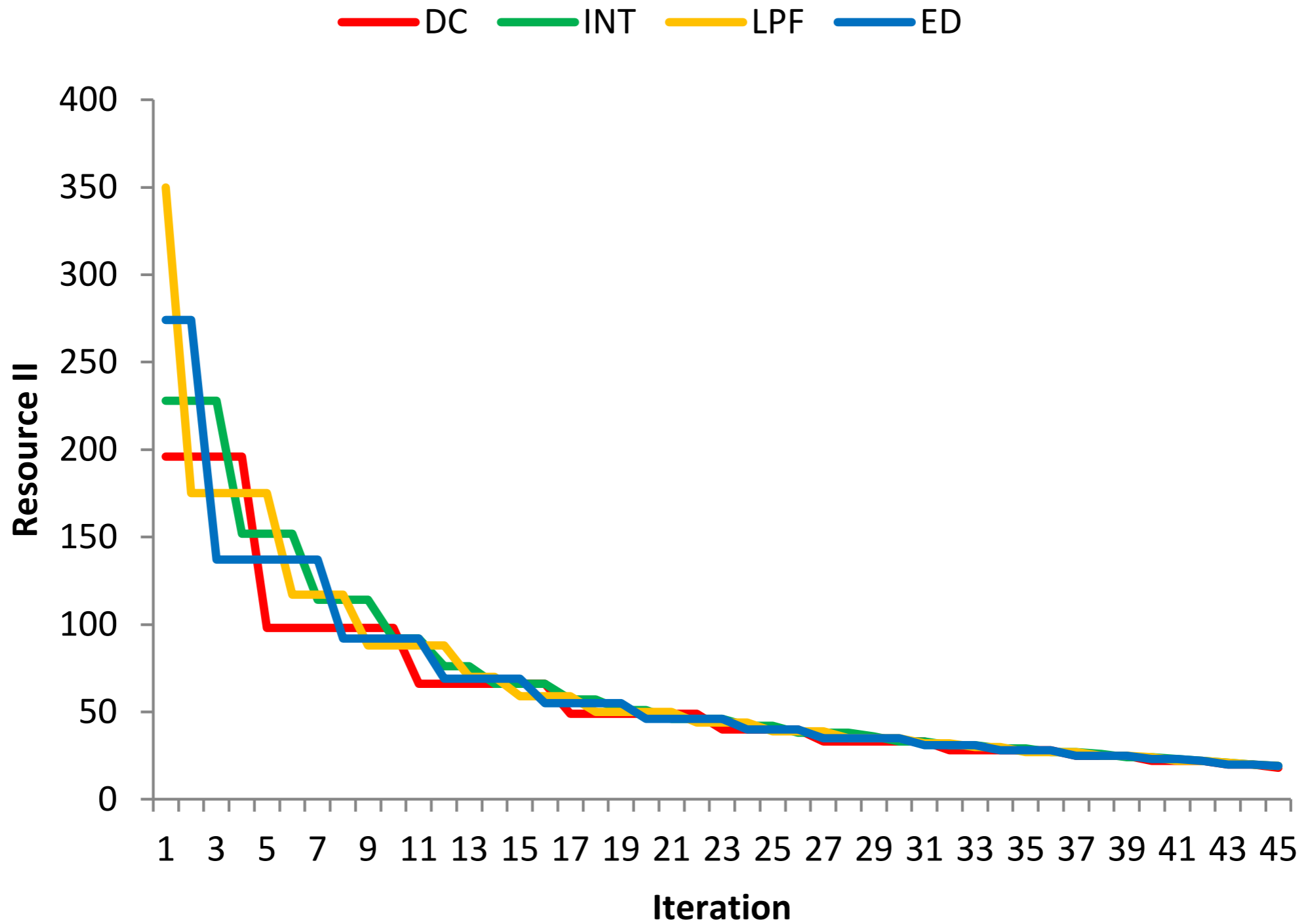
Resource Allocation Algorithm

- Allocate minimal resources to each kernel
- Do
 - Find kernel(s) limiting performance
 - Translate performance through port rates
 - Increment resources of these kernels
- Until
 - Resource exhausted
 - Limiting kernel(s) at recurrence II
- Provably optimal algorithm

Allocation Progression

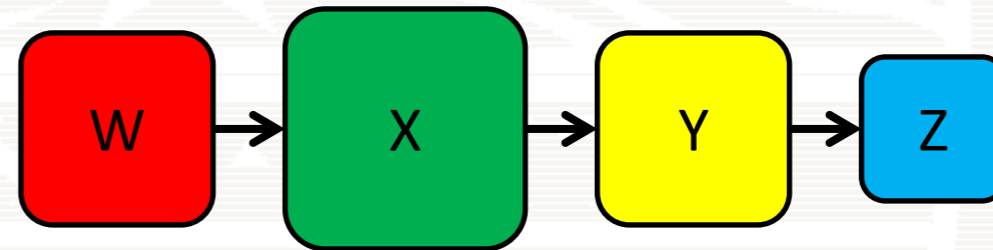


Initiation Interval Progression



Kernel Placement

Resource allocation:

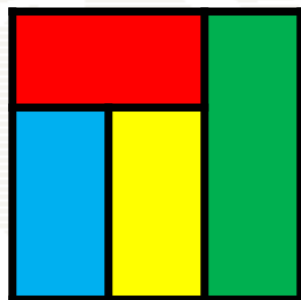


Simulated annealing to arrange allocated resources

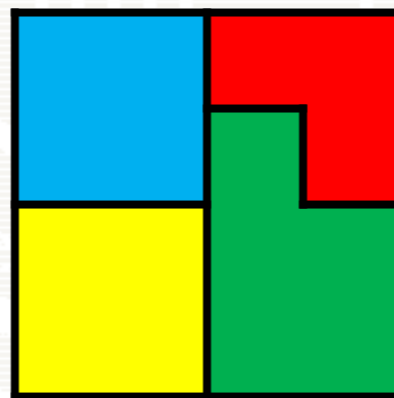
Cost function

- Maintain cohesion of individual kernels

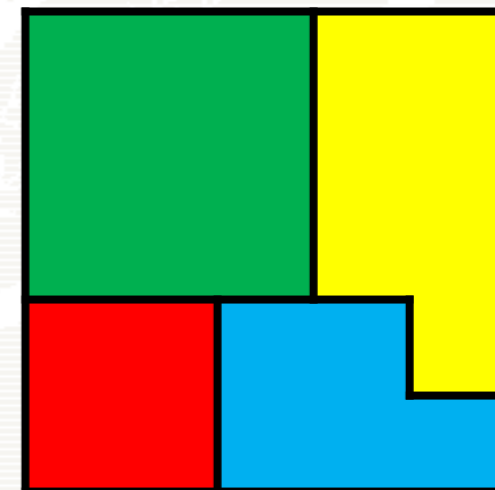
- Maintain abutment of communicating kernels



small device



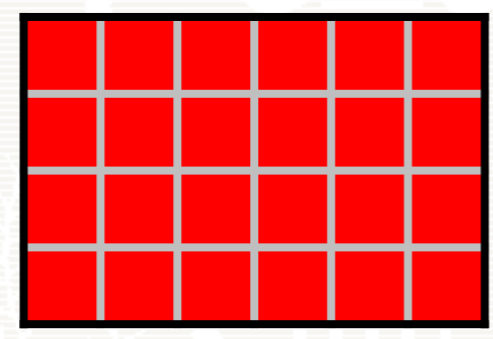
medium device



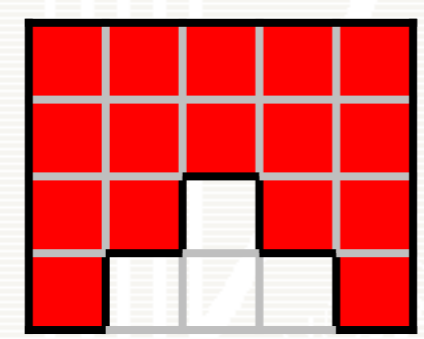
large device

Cost Function

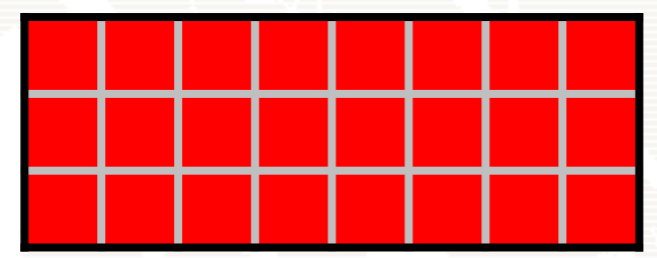
Kernel Cohesion



Perimeter 20



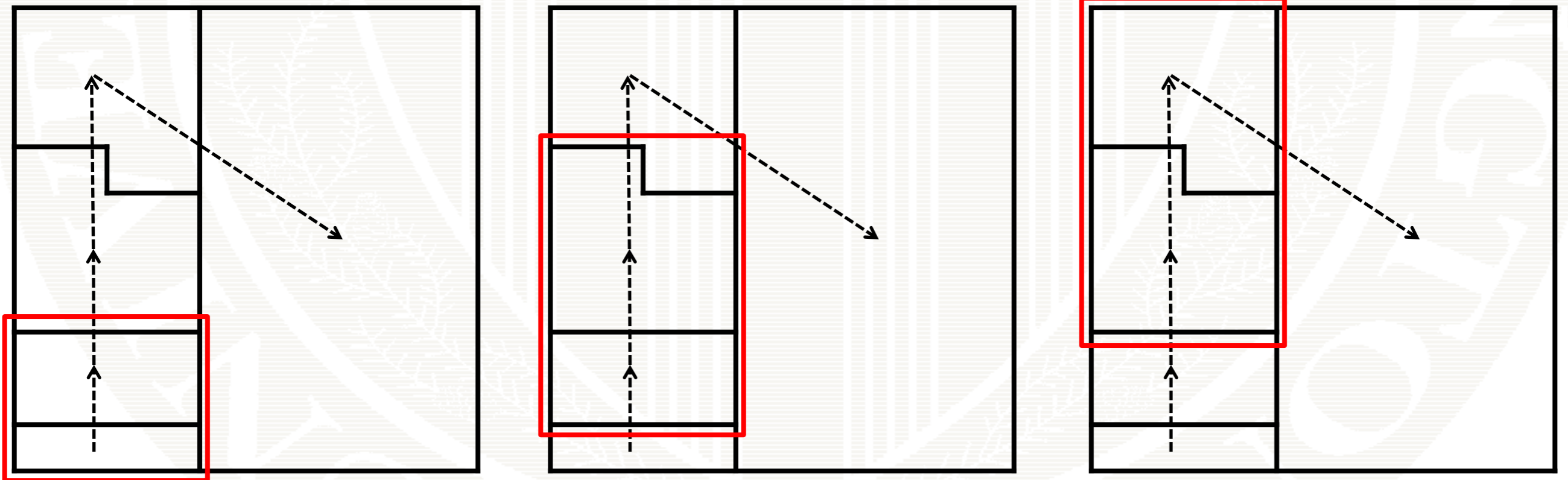
Perimeter 22



Perimeter 22

Cost Function

Extend metric to inter-kernel communication



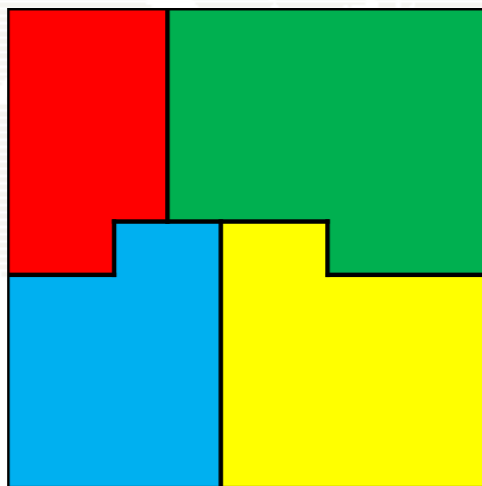
Placement Results

- Runtime dwarfed by other parts of the tool chain
 - Wavelet application completes in less than a minute
 - Many options for optimization – incremental cost function

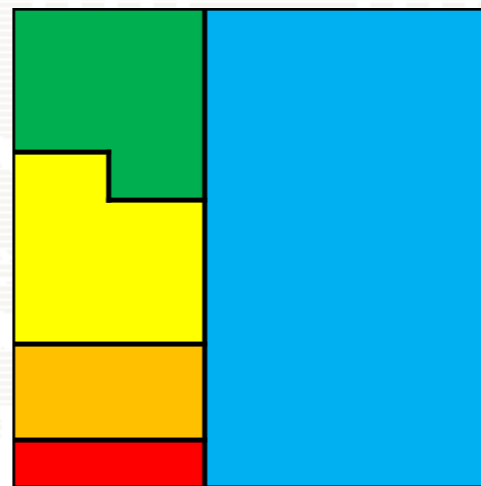
App	Min Cost	Generated Cost	Cost Ratio	Average Wirelength	Max Wirelength	Kernels
DWT	100	108	1.08	1.0	1.0	3
PET	44	44	1.00	1.0	1.0	2
Bayer	176	182	1.03	1.0	1.0	5
IPL	156	164	1.05	1.0	1.0	4
Wavelet	476	522	1.10	1.2	5.0	18

CAD Tools for Enhanced CGRAs

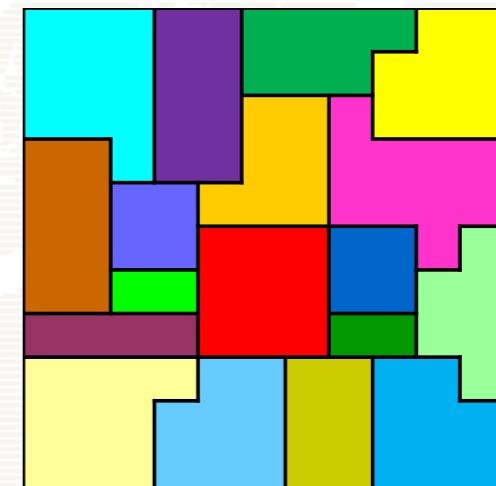
- Builds on capabilities of previous work
- Reduced design effort
 - Provides greater flexibility for the programmer
 - Maximizing performance for a given device
- A path toward processor array tools
 - Applicable to floorplanning these devices as well
 - Leverage greater independence between device sections



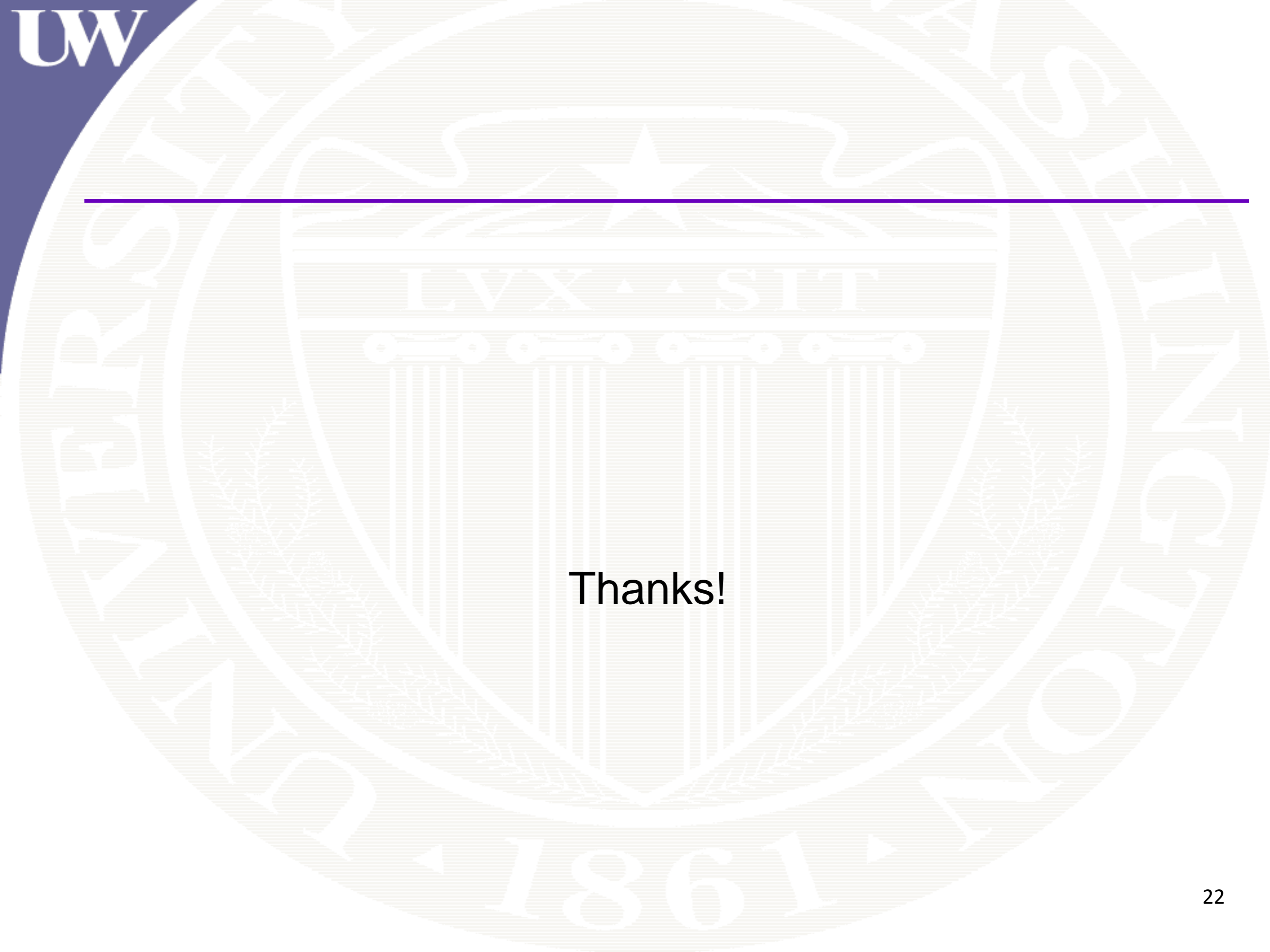
Camera Pipeline



Bayer



Wavelet



Thanks!