Imperial College London ADAPTIVE SEQUENTIAL MONTE CARLO APPROACH FOR REAL-TIME APPLICATIONS

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Introduction

- Sequential Monte Carlo (SMC) methods: estimate states of dynamic systems using weighted particles.
- Adaptive real-time approach: analyse run-time workload for

Results

- Platform: Altera DE4 development board with a Stratix IV EP4SGX530 FPGA running at 100MHz.
- Example application: localisation of mobile robots.
- dynamic task allocation to processors on FPGA to improve energy efficiency.
- Example: dynamic energy consumption of robot localisation is reduced by up to 70% without affecting solution quality.

Motivation and Objective

- Real-time systems are often energy constrained.
- Events often occur at regular intervals for real-time applications.
- Objective: reduce energy by exploiting slack time when system is idle.

Sequential Monte Carlo Methods

- X_t State of the system at time t.
- Y_t Observation of the system at time t.
- $\{x_t^i | i=1,...,P\}$ A set of P particles representing X_t .
- $\{w^{*i}_{t} | i=1,...,P\}$ Associated weights of the set of particles.



More particles are need for global positioning than local tracking.



• Computational complexity: reduced as the size of particle set changes dynamically.





Adaptive SMC Approach

- Sampling and Importance: particles are distributed to N processors for parallel processing.
- Reduction: particles with low weight are eliminated, i.e. workload is reduced.
- Resampling: the set of particles are restored if the particle count (P_t) drops below a threshold (M).
- Resource allocation: particles are distributed to processors which are deactivated after computation finishes.



- Dynamic energy consumption: reduced by 35-70%.
- Timing constraint: satisfied.





- Estimate states of dynamic systems: weighted particles.
- Dynamic workload: run-time task allocation to processors.
- Reduced energy: timing and quality of results maintained.

[1] M. Happe, E. Lubbers, and M. Platzner, "A Multithreaded Framework for Sequential Monte Carlo Methods on CPU/FPGA Platforms," International Workshop on Applied Reconfigurable Computing, 2009.

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