Field-Programmable Logic and its Applications

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Fault Detection and Avoidance of FPGA in Various Granularities

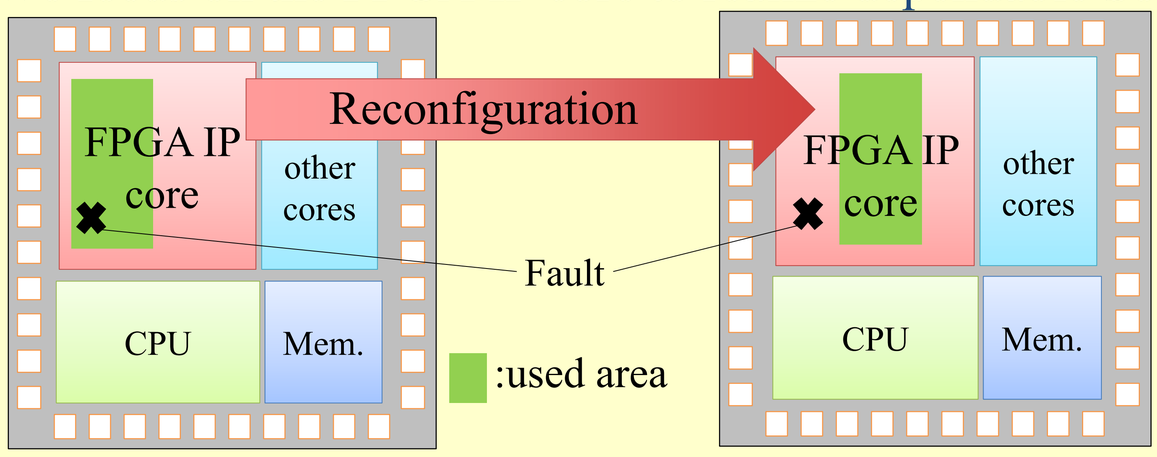
Kazuki Inoue, Yuki Nishitani, Motoki Amagasaki, Masahiro Iida, Morihiro Kuga, Toshinori Sueyoshi

Kumamoto University, Japan

1. Introduction

Fault Tolerant Technique with Reconfiguration

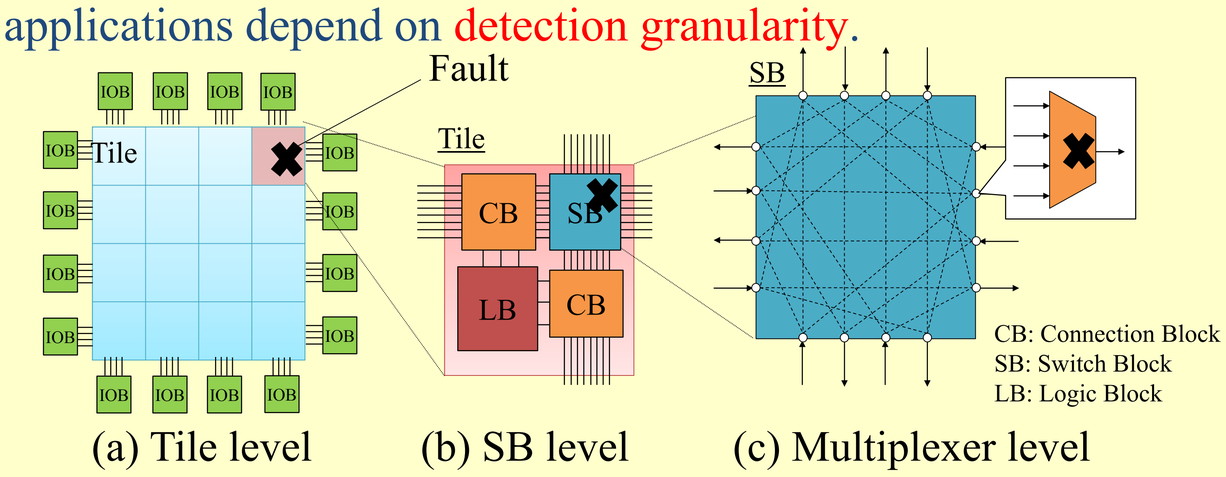
A Fault Tolerance is crucial for SoCs in dependable systems.
We focus on the FPGA IP core to realize dependable SoCs.



FPGA can easily recover from faults using reconfiguration.

Key points of Fault Tolerant technique

Recovery (detection and avoidance) time and performance of applications depend on detection granularity.



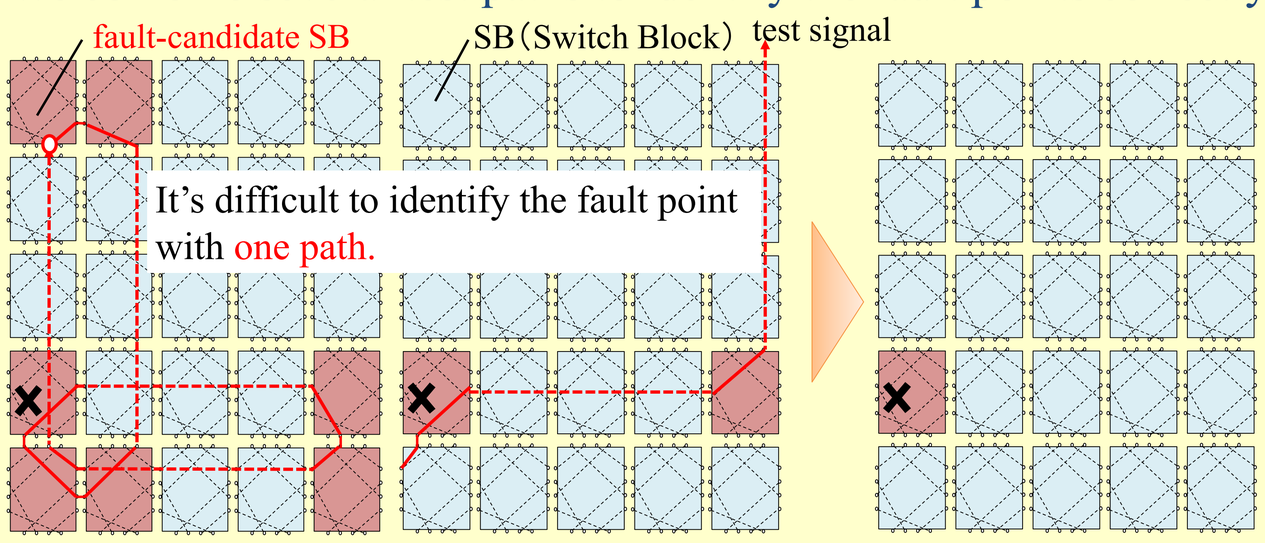
Short	Detection Time	*Long*
Long	Avoidance Time	*Short*
Low	Performance	*High*

We propose fault detection and avoidance technique for global interconnects in various granularities.

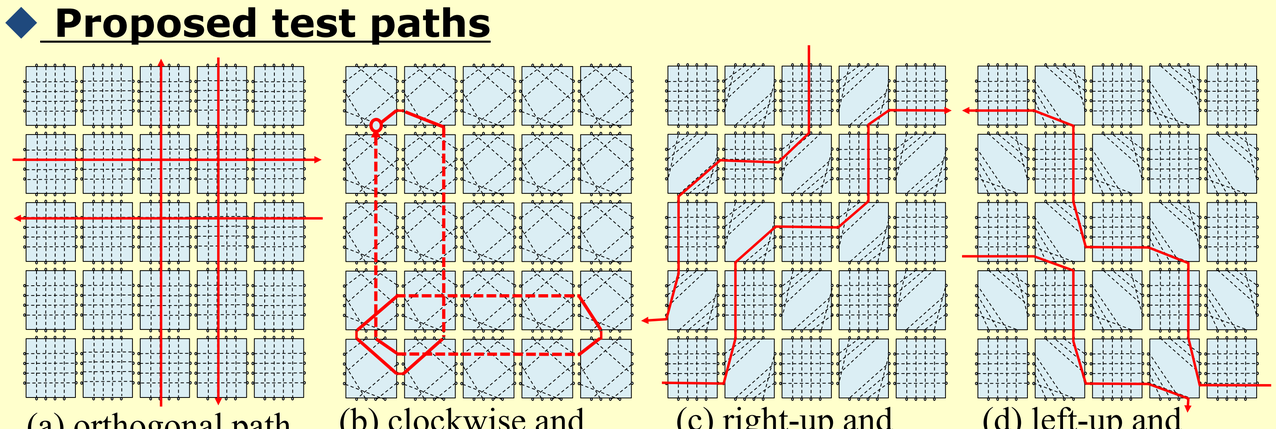
2. Fault Detection Technique

Key Idea of fault-detection

We combine several test paths to identify the fault points correctly.



Proposed test paths

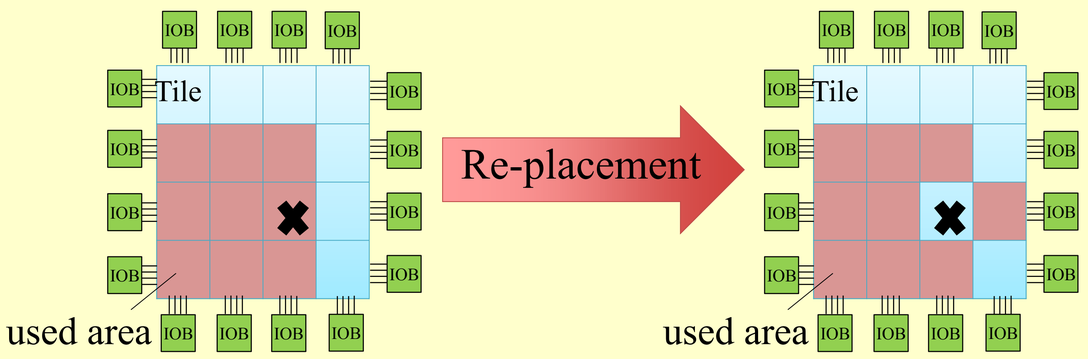


- Test paths (a) and (b) were proposed in previous work.
  They achieved 100% fault coverage for interconnect testing.
- (c) and (d) are newly prepared for fault diagnosis in this work.

3. Fault Avoidance with CAD tools

Fault Avoidance in Placement phase

We modified the placer in VPR5.0 to avoid fault tiles .



Modified placement flow

Initial placement → Fault check → Try swap → Fault check → Cost update → END

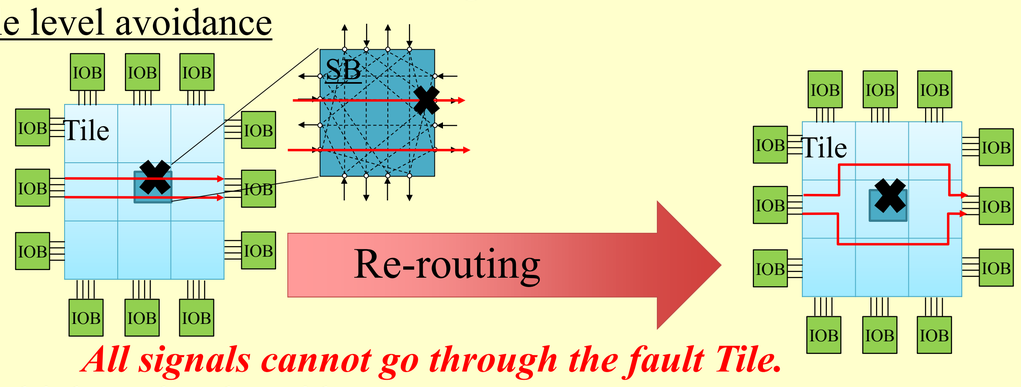
Retry until no fault points are used.

Re-placement is performed only in Tile-level avoidance.

Fault Avoidance in Routing phase

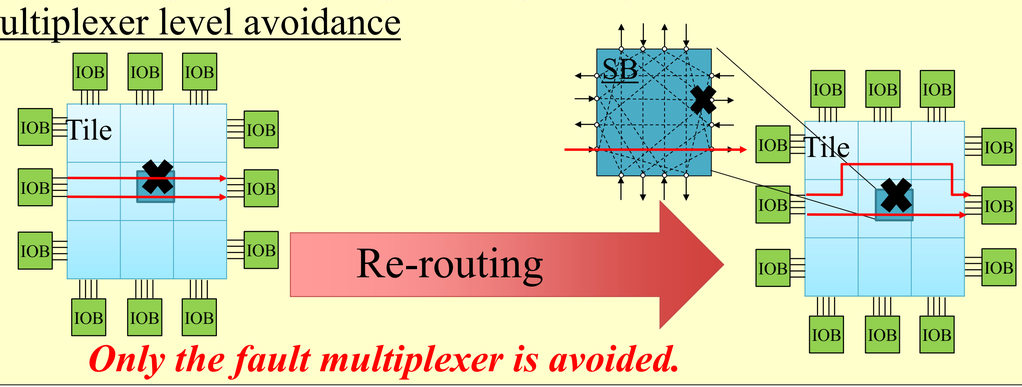
We modified the timing-driven router in VPR5.0.

Tile level avoidance



All signals cannot go through the fault Tile.

Multiplexer level avoidance



Only the fault multiplexer is avoided.

4.Evaluation

Evaluation Conditions

Target Device

Item	value
Array size	16×16
Logic block	4×6-LUT
Channel width	48
# of I/O pins	128
Configuration bits	136,896

※designed by 65 nm process technology

Target Fault

Stuck-at single fault at the SB

Detection Method

Method（1）: Test paths (a) and (b)
Method（2）: Test paths (b), (c), and (d)

Avoidance Method

Tile-level: Re-placement and re-routing
Multiplexer (MUX) -level: Re-routing only

Evaluation Results

Results of fault detection

Detection method	Method (1)	Method (2)
detection time (clock cycle)	798,992	1,122,970
# of fault tiles (worst/best)	44/4	7/1
# of fault multiplexers (worst/best)	144/12	14/1

The paths of Method (2) detected the fault SB correctly with 40% additional time compared to Method(1)!!

Circuit delays affected by fault-avoidance[ns]

	No fault	Method (1)		Method (2)	
avoid . level		Tile	MUX	Tile	MUX
C6288	96.7	N/A	96.6	100.3	96.2
cordic	103.4	N/A	102.2	111.4	93.9
ex4p	46.4	N/A	46.7	49.1	47.4

Avoidance time[s]

Circuit	Tile	MUX
C6288	4.25	0.94
cordic	3.60	0.87
ex4p	3.28	0.38

N/A: Implementation failed.

# of fault-candidates Method (1) : 25 Tiles, 48 MUXs, Method (2): 2 Tiles, 2 MUXs.

MUX-level avoidance achieved high success ratio of implementation and performance same as no fault FPGA in short avoidance time!!