IMPLEMENTATION TECHNIQUES FOR EVOLVABLE HW SYSTEMS: VIRTUAL VS. DYNAMIC RECONFIGURATION

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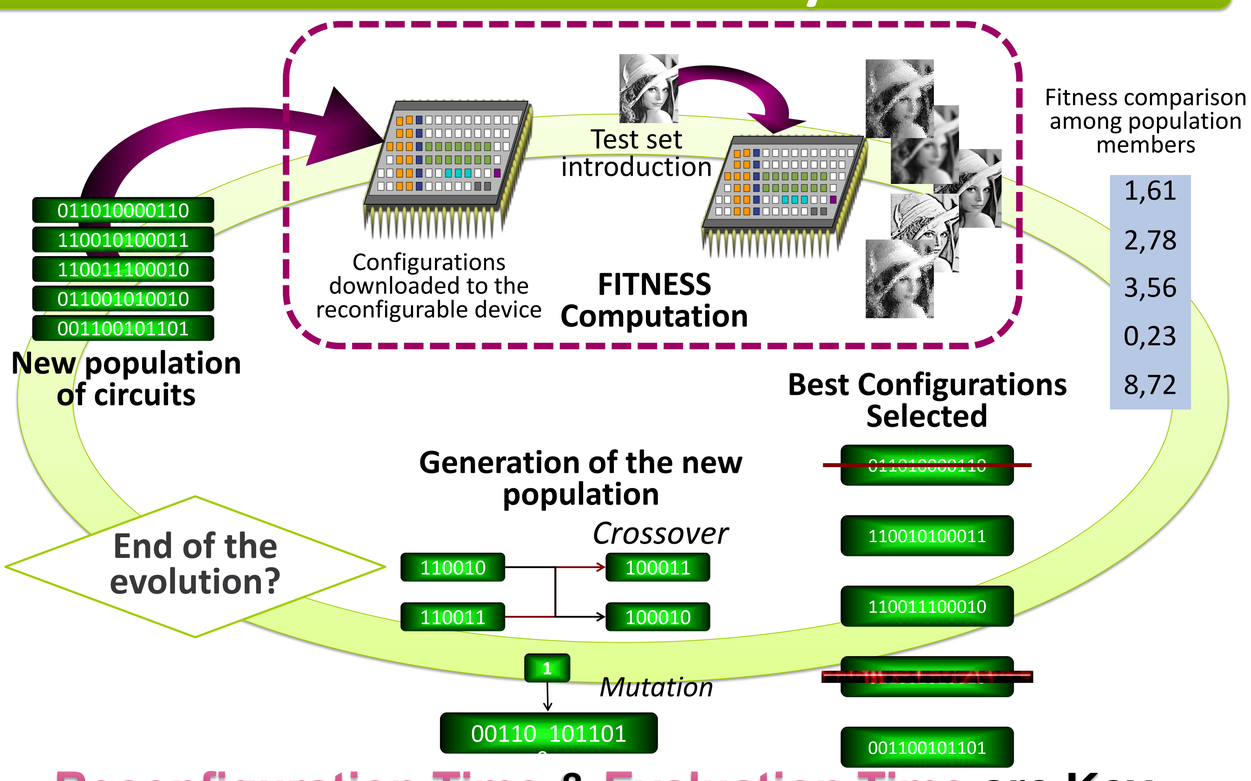
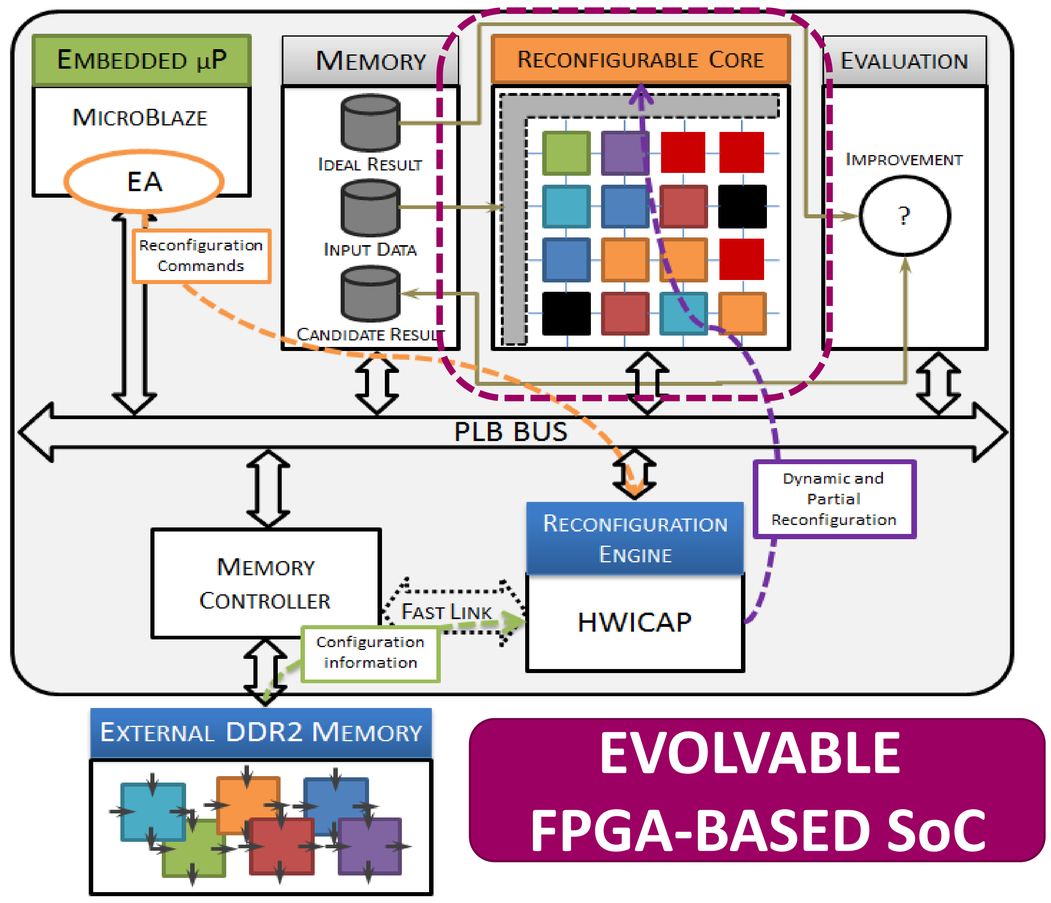
Adaptive hardware requires some reconfiguration capabilities. FPGAs with dynamic partial reconfiguration (DPR) support pose a dilemma for system designers: whether to use native DPR or to build a virtual reconfigurable circuit (VRC) on top of the FPGA which allows selecting alternative functions by a multiplexing scheme. This solution allows much faster reconfiguration, but with higher resource overhead. This paper discusses the advantages of both implementations for a 2D image processing matrix.

Evolvable Hardware Systems



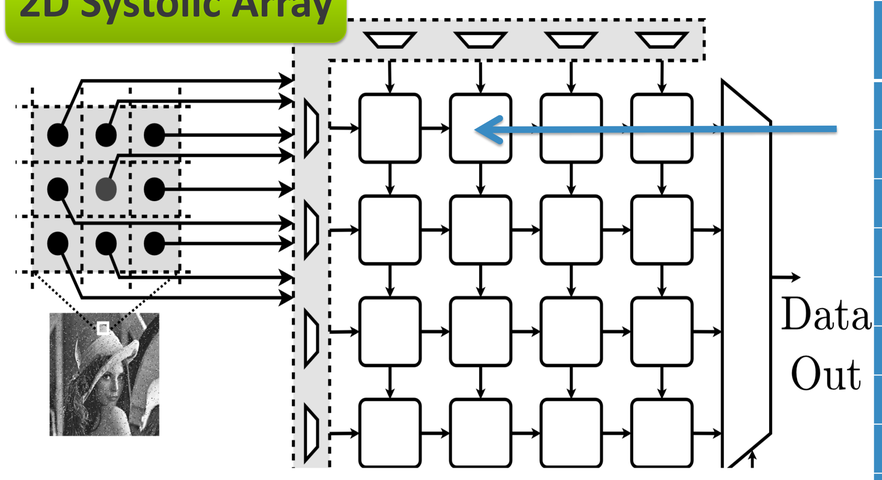
Reconfiguration Time & Evaluation Time are Key Factors for Perfomance



EVOLVABLE FPGA-BASED SoC

Processing Array

2D Systolic Array



PE library

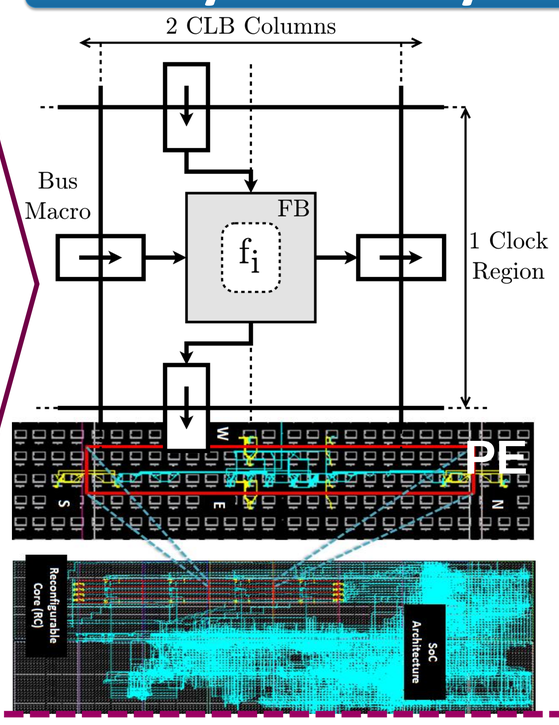
ID	Function
0	x + y
1	x << 1
2	x +$_s$ y
3	(x + y) >> 1
4	255
5	x >> 1
6	x
7	max(x,y)
8	min(x,y)
9	x −$_s$ y

MODULARITY

REGULARITY

Scalable

Dynamically Reconfigurable Core



RECONFIGURATION TIME

PROCESSING SPEED

AREA OVERHEAD

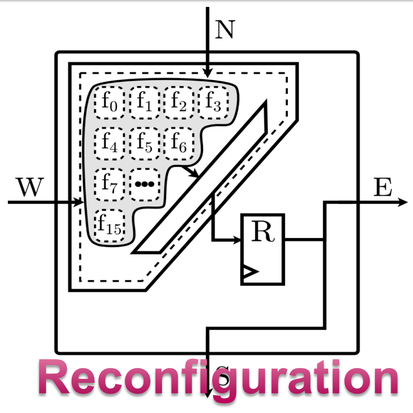
But...

EXTRA AREA FOR RE

BUS-MACRO OVERHEAD

Fast ICAP operation with relocation: 200 MHz

Virtual Reconfigurable Circuit (VRC)



RECONFIGURATION TIME

AREA OVERHEAD

PROCESSING SPEED

Reconfiguration => writing a big register which controls a set of multiplexers

Implementation Results

Version	Module	Slices	Slice Regs	Slice LUTs	LUTRAM	DSP	BRAM
RA	Component	5763	12931	11276	1518	0	38
	Array	1280	5120	5120	1280	0	0
	Misc	1101	1932	1932	64	0	12
	HWICAP	1615	2765	2344	145	0	9
	Mem. Ctrl	1767	3114	1880	29	0	17
VRC	Component	2791	4224	5472	128	0	12
	Array	1096	215	2539	0	0	0
	Misc.	1567	3676	2300	128	0	12

Virtex5 LX110T

Task	Time (μs) RA@200MHz	VRC@100MHz
Reconfig. (1 PE)	15.92	0.4
Reconfig. (3 PE)	69.61[a]	
Filtering	82.12	163.84
Total evolution	122	132

- **(1+λ) Evolution Strategy** with 1 parent and λ offspring (Inspired from CGP).
- 4×4 core for **image noise filtering**
- Fitness Function: Mean Absolute Error (MAE)
  - PE size = 2 CLB (W) × 1 clock region (H) (40 CLBs)

Latest Results: 10 CLBs per PE

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