High-Level Aging Estimation for FPGA-Mapped Designs

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Purpose

- Introduce a high-level yet device-level relevant aging estimation model
  - Suitable for FPGA architectures
  - Estimates the application information (usage)
    - In addition to device-level information

- Build an FPGA aging estimation tool
  - Based on the high-level model
  - Infer the necessary information from the design tools of the FPGA
  - Can be used directly by FPGA users
    - Without the need for device-level details
Outline

- Motivation
- Aging model abstraction
- FPGA aging estimation tool
- Experimental results
- Conclusion
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FPGAs and Technology Scaling

- Why scaling down ➔ The need for circuits that are:
  - High-performance, Low-power-consumption, Portable and Low cost

- FPGAs are in the front line to benefit
  - High volume, regular, and high scalable structure
  - High performance demands for digital and mixed-mode analog circuits

- Examples of state-of-the-art FPGAs:
  - Xilinx Virtex-7
    - 28nm - based process technology
    - Up to 2M logic cells
    - 600+ MHz operating frequency
  - Altera Stratix-V
    - 28nm - based process technology
    - Up to 1.19M logic elements
    - 600+ MHz operating frequency

- However downscaling comes with reliability challenges
Reliability challenges of downscaling: Aging

- **BTI:** Bias Temperature Instability
  - Negative BTI (NBTI) affects PMOS
  - Positive BTI (PBTI) affects NMOS
    - Appears in high-κ / metal gate materials

- **HCI:** Hot Carrier Injection

- Main effects:
  - Increase the threshold voltage ($V_{th}$)
  - Decrease the carrier mobility
  - Slow the switching speed

- The combination of these effects is usually called *(transistor aging)*
Device-Level Aging Models

- Main factors affecting $\Delta V_{th}$ induced by BTI and HCI:

  - **BTI**: $\Delta V_{th}$ depends on
    - $t$: time (circuit age in seconds)
    - $Y$: duty cycle (the ratio of the stress time to the total time)
    - $T$: temperature (Kelvin)

  - **HCI**: $\Delta V_{th}$ depends on
    - $t$: time (circuit age in seconds)
    - $\alpha$: activity (number of activations in one cycle)
    - $f$: operational frequency. The factor $\alpha \times f$ is known as the activity rate (AR)
    - $T$: temperature (Kelvin)

[Bravaix 2009, Takeda 1983]
FPGA Users and Aging Estimation

- FPGA users cannot use device-level aging models.
- Aging also depends on the mapped design, resource usage.

**FPGA Aging Model (BTI, HCI)**

- **Application** (Gate level netlist) - Available
- **Physical Design** (Which resources used by mapping) - Partially available
- **FPGA device information** (Circuit-level information of slices, LUTs, …etc) - FPGA Lib info - Vague (mostly proprietary)

**Overall ∆delay after x years for the mapped circuit**
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Available information from the FPGA tools

- All information is provided at node level

- One node (black box circuit) can be
  - LUT
  - Slice flip flop
  - Routing path through switch matrices
  - ...

- Information include:
  - Delay of paths inside a node (Timing tool)
  - Node switching activity (Power tool)
  - Node dynamic power (Power tool)
Different sub-circuits (nodes) in the FPGA

Information is available at nodes’ input and output
Aging Model Abstraction (1)

- Each path through the node is represented by a chain of blocks
- Each block contains an inverter
  - To consider the effect on both NMOS and PMOS type of transistors

- Two adjustment steps:
  - **First (emulate the delay)**
    - # of blocks = path delay / delay of one block
    - The delay of one block depends on the technology node used
Aging Model Abstraction (2)

Information is available at nodes’ input and output

Second (estimate internal details): linearization for estimating internal

- Signal probability (SP) for BTI estimation, \( Y = 1 - SP \) (NBTI) , \( Y = SP \) (PBTI)
- Activity rate (AR) for HCI estimation

\[
SP_j = \begin{cases} 
SP_i + j \frac{|SP_{out} - SP_i|}{m-1}, & \text{if } SP_{out} \geq SP_i \\
SP_i - j \frac{|SP_{out} - SP_i|}{m-1}, & \text{else}
\end{cases} 
\quad j = 1, 2, \ldots, m-1
\]
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FPGA Aging Estimation Tool: Overview

User Design

FPGA Tools

Timing Report

Power Report

XDL file

XDLRC file

Logic Simulation (VCD file)

Power Report

Nodes Extraction

Temperature Profile Calculation

Temperature Per Node

Activity Rates Calculation

Signal Probabilities Calculation

Signal Probabilities (Duty cycle)

Activity Rates

Aging Estimation (HCl, BTI)

1. Delay Degradation
2. Life time change

1. Paths
2. Nodes
3. Pre-aging delays

Usage

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Temperature Profile Calculation (1)

- **Floorplan generation**
  - Die dimensions
  - Chip resources (XDLRC file)
  - \( X \times Y \) number of tiles
  - Group each set of tiles in one block

- **Power trace**
  - Using power report of the design
    - Needs activity file from logic simulator
  - Dynamic power
    - Find physical location for each component
    - Assign component’s power to respective blocks
  - Leakage power
    - Given as one value for whole FPGA
Temperature Profile Calculation (2)

- **Leakage Power**
  - Equaly-distributed
  - Not accurate (thermal camera)

- **Leakage Distribution Model**
  - Based on leakage-temperature loop
  - Original leakage redistributed

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**HotSpot**

<table>
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<tr>
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**Original Leakage**

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**Temperature Distribution Model**

**XDLRC File**

<table>
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</table>

**XDL File**

**Per-node Temperature Calculation**
FPGA Aging Estimation Tool: Overview

1. Paths
2. Nodes
3. Pre-aging delays

1. Delay Degradation
2. Life time change

Usage

1. Timing Report
2. Power Report
3. XDL file
4. XDLRC file
5. Logic Simulation (VCD file)
6. Power Report

Nodes Extraction

Temperature Profile Calculation

Temperature Per Node

Activity Rates Calculation

Signal Probabilities (Duty cycle)

Signal Probabilities Calculation

Aging Estimation (HCl, BTI)
Aging Estimation

Step 1
Finding the amount of change in node’s delay due to aging ($\Delta d_{node(BTI)}$ and $\Delta d_{node(HCI)}$)

Step 2
Calculating, for each node, the new delay due to aging ($d_{0node} + \Delta d_{node}$)

Step 3
Finding the aged-circuit critical path’s delay ($d_{critical}^\sim$), and compare it to the fresh-circuit critical path’s delay ($d_{critical}$)

The performance degradation due to aging
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Experimental results
- Validation of the proposed abstraction
- Validation of the thermal model
- Tool usage: Case Study

Conclusion
Validation of the Proposed Abstraction

- HSPICE simulation for different types of node
- More than 90% match in the trend
- Example 2-input LUT:

\[
\begin{align*}
&SP_0 (\ast 0.1) \\
&SP_0 (\ast 0.1) \\
&\text{Configurations (for each, SP}_1 = 0.1, 0.2, \ldots, 0.9) \\
&\text{SP output (mapped according to HSPICE results)}
\end{align*}
\]
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Thermal Model Validation (1)

- A thermal (infrared) camera is used
  - Accuracy ±1 °C
  - Attached to Virtex-5 vlx110t FPGA
  - After removing the packaging (no heatsink, no heatspreader)

- Two circuits under test:
  - 8-bit FIR filter at 150 MHz
  - 128-bit AES encoder at 300 MHz

- Do a comparison between:
  - The Thermal Model and
  - The Thermal Camera
Thermal Model Validation (2)

AES Encoder

FIR Filter
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Case Study: Influence of Mapping and Optimization Algorithms (1)

- Three cases:
  - (1) Area optimization, (2) Speed optimization
  - (3) Force placement with speed optimization

- Different ITC’99 test bench circuits in addition to an FIR filter
  - Virtex6-vlx75t (fit all the circuits)
  - Mapped only to LUTs and flip-flops for fair comparison

- 10000 vectors are tested for each experiment to calculate
  - Signal Probabilities (SP), Signal Activities (AR)

- Worst case NBTI and HCI is set
  - For SP = 1 (PMOS transistors always ON worst case NBTI)
  - For AR = 500 MHz (maximum frequency $\Rightarrow$ worst case HCI)
Case Study: Influence of Mapping and Optimization Algorithms (2)

NBTI

<table>
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<td>FIR Filter</td>
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HCI

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<tbody>
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<td>FIR Filter</td>
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<td>b05</td>
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</tbody>
</table>

- **Speed optimized**
- **Forced placement**
- **Area optimized**
A small change in the degradation rate has a significant effect on the lifetime.
Lifetime Enhancement Compared to Worst Case

**NBTI**

- **FIR Filter**
- **b14**
- **b12**
- **b11**
- **b05**
- **b04**

**HCI**

- **FIR Filter**
- **b14**
- **b12**
- **b11**
- **b05**
- **b04**

Legend:
- Speed optimized
- Forced placement
- Area optimized

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- Transistor aging is a major reliability issue. Mainly due to
  - Bias Temperature Instability (BTI)
  - Hot Carrier Injection (HCI)

- Accurate aging estimation requires
  - Device info, used resources (mapping), and user application (workload)

- Developed an FPGA aging estimation tool
  - Can be used directly by FPGA end-users
  - Infers device info from FPGA reports (timing, power, etc.)
  - Considers mapping and user application

- Aging of FPGA depends on:
  - (1) The target FPGA chip (2) the application and (3) how it is mapped
References


Thanks for your attention